High-speed dynamic spectrum data acquisition system based on linear CCD

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High-speed dynamic spectrum data of transient detection has become the major means of access to transient information. However, in terms of the characteristic of spectral data excessiveness and transience in the dynamic spectral detection system, the linear charge-coupled device (CCD) used in the system should have real-time-output and match the high-speed data storage equipment. Based on the transient spectrum characteristic, we introduce a high-speed dynamic spectrum data acquisition system with a high-linear array CCD. Through the field of programming gate array, the system provides an accurate driving clock for CCD and generates the control signals for analog-to-digital (A/D) conversion, storage, and transmission. Finally, the collected data by the peripheral component interconnect bus are summarized and filtered in the host computer. The results show that the CCD can stably work with a 40-MHz clock, and the frame scanning frequency can achieve 73 KHz. This design can remarkably complete the real-time measurement of the denotation transient temperature and achieve high-speed spectral information collection and storage with high accuracy and frame scanning frequency. It can be applied to other transient information acquisition.

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In the fields of measurement on the temperature characteristics and correlation properties of high-temperature gas and plasma, the detection of dynamic spectrum has been widely applied to detecting facilities. Compared with other measurement methods, dynamic spectrum has outstanding advantages, such as a nondestructive flowing-field, a simple system without an external excited source, and relatively precise results. Under explosive detonation, spectral radiation is an unavailable parameter because of its brief time and strong transience. Therefore, the acquisition and storage of spectral information seem particularly important in the study of the regularities of new solid explosives in the national defense industry[1−7].

Following the constant improvement in manufacturing technology, many charge-coupled devices (CCDs) have been used in the signal detection area, especially in spectrum detection. Its distinctive advantages in performance have carried out concurrent multi-wavelength scanning, replaced the previous complex machine scanning devices, decreased the error sources, and enhanced detection accuracy[8]. Furthermore, due to its advantages of sensitivity, signal-to-noise ratio (SNR), and wide dynamic range, the CCD has been widely applied to detecting facilities. The system of measuring a dynamic spectrum requires high-order accuracy and high tensity resolution. Therefore, the massive output data from the CCD and the datas high export rate from the CCD constitute a large mismatch in the transfer speed between the general transmission module and the CCD.

For the sake of solving the anterior issues, in this letter, we present an acquisition system based on the field of programming gate array (FPGA) and the larger-capacity double data rate (DDR) synchronous dynamic random access memory (SDRAM) using the high-speed linear CCD as an image sensor. EP2C8T114C8 is used as the main control chip. Combined with the technology of the peripheral component interconnect (PCI) bus, this system carries out real-time acquisition and storage of spectral information, and shows the curve diagram of the spectral intensity by utilizing the host computer handling the gathered data.

Currently, the application of FPGA technology has several prominent advantages, e.g., convenient programming, excellent real-time performance, flexible design, and interface functions using software. Therefore, FPGA is chosen as the master chip to coordinate the various modules in the system. Using the master chip, i.e., the FPGA, the system can easily perform control sequence and data transmission, and reliably achieve sampling and storage[9]. The main function module consists of four parts: driving schedule of CCD, CCD-mode timing of analog/digital (AD), DDR SDRAM controller module, and PCI controller.

When the system begins to operate, the external pulse triggers the AD chip. During sampling, the collected data from AD are stored in a large DDR SDRAM by the FPGA controller. After sampling, the host computer reads data from DDR SDRAM through the PCI bus. Finally, data is analyzed using software, and the spectral intensity curve is presented in the period of explosion. The system block diagram of high-speed spectrum acquisition is presented in Fig. 1, including spectral acquisition, storage and transmission, and data processing.

Spectral signal sampling is composed of high-speed linear CCD and AD. Figure 2 shows the main functional

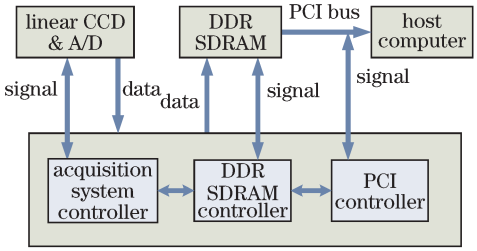

Fig. 1. System block diagram of high-speed spectrum acquisition.

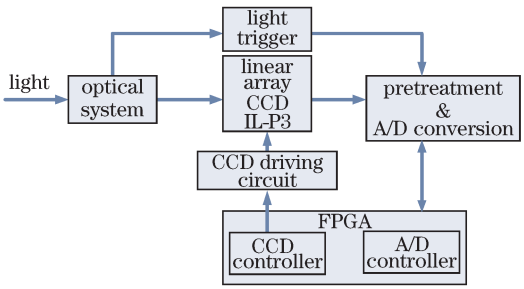

Fig. 2. Functional diagram of spectral acquisition.

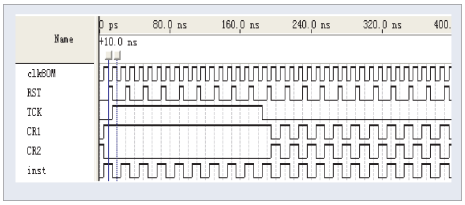

Fig. 3. Simulated time scheduling of CCD.

diagram of this part.

CCD, which transforms from an optical signal to an electrical one, is one of the general imaging sensors in a spectral detecting system and can work stably under the high-speed condition. The correct timing-driven design is a key aspect in working consistently with CCD in natural status because it directly affects the quality of the operation stability of the CCD. Here, we use the IL-P3-type linear CCD (DALSA Co.), which has a single output of 40-MHz data rate, a line rate of 73 KHz, and high sensitivity with a responsivity of 43 V/(μJ·cm^2). Incorporating the advantage of very-high-speed integrated circuit hardware description language, the driven pulses are designed based on the analyzed results from the timing of the CCD. The simulated time scheduling is shown in Fig. 3.

To store and deal with the collected analog signals, converting the analog signal outputted from the CCD into a digital situation is required. Under the condition of satisfying the precision of AD conversion, a high-speed sampling rate is very important to obtain spectral information. High-quality spectral information can be obtained using the technique of correlated double sampling (CDS), by which the system eliminates noise in the effective signal and decreases the reset noise in the linear CCD.

Designing and debuging the CDS circuit with discrete devices is complicated, and thus an integrated chip AD9840 (Analog Devices Inc.) is applied. AD9840A is a complete 10-bit 40 MSPS CCD signal processor that includes an input clamp, CDS, digitally controlled variable gain amplifier (VGA), and black level clamp. Through the aid of three connection signals, namely, SLOAD, SCK, and SDATA, the CCD signal processor can configure its internal register to a certain mode, enabling the CCD sample the suitable spectral signal. The CCD-mode timing of AD is shown in Fig. 4.

For the sake of analysis and treatment of transient spectrum information, the system requires the real-time storage of high-speed and large data from the anterior AD. DDR is an evolutionary memory technology based on SDRAM. DDR SDRAM access is twice as fast as that of SDRAM because DDR data transfers occur on both edges of the clock compared with SDRAM, which transfers data only on the rising edge of a clock. Consequently, DDR can transfer data at up to 2133 MB/s and can completely satisfy the requirement of the system. The gathered data from AD are transferred to FPGA, where the dataflow is buffered and converted. Dataflow is then transferred to the memory cell in the DDR to analyze the information on the spectrum. DDR, SDRAM MT46V32M16 made by Micron Co. is used in this system, which has a capacity of 512 M and meet the storage requirements of the system.

The DDR controller mainly contains four modules: control interface module, data path module, command interface module, and DLL module. Figure 5 highlights the internal control modules.

The main function of the control interface module is to save and decode the commands from the user. The interface module may support some conventional commands, such as NOP, WRITEA, REA-DA, REFRESH, PRECHARGE, and LOAD-MODE. Through the control interface module, the signals of the command and address are transformed into the command interface module at

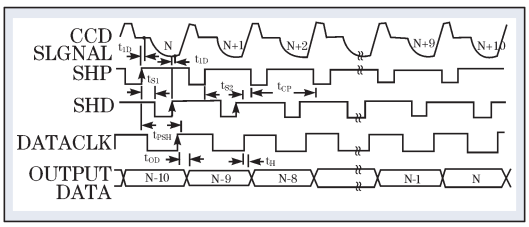

Fig. 4. CCD-mode timing of AD.

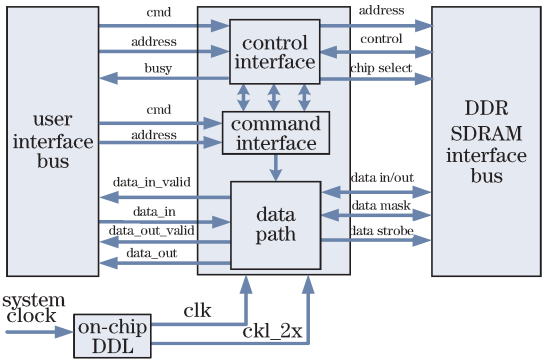

Fig. 5. Internal control modules of DDR SDRAM.

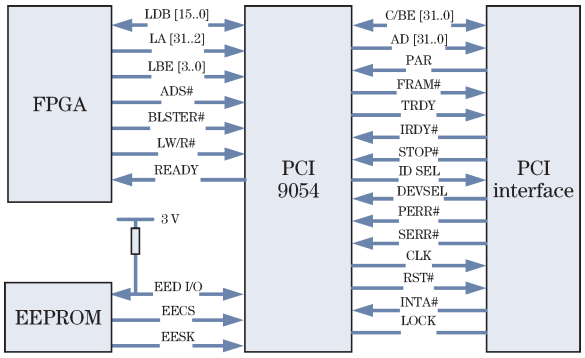

Fig. 6. PCI peripheral interface circuit.

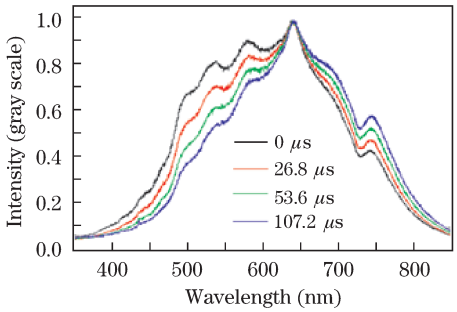

Fig. 7. Dynamic spectrum of detonation radiation.

the same time. The signals of the address gating are then generated.

The command interface module receives decoded commands from the control interface module and executes the corresponding operations in the SDRAM, including the front commands. In this module, a simple arbiter arbitrates the requirement between the command and refresh. The requirement of refreshment has priority over others. There is a register of 16 bits in the refresh counter to refresh automatically.

The data path module can supply the data pathway between DDR and user interface. By allocating the path width, it can support data widths of 16, 32, and 64. Burst lengths can be set to 2, 4, and 8. The data width of the data path is twice that of DDR SDRAM. The operations were conducted both in the rising and falling edges. At the same time, DQS signal was generated by the data path module informationally, i.e., data path module gated the data to be written in DDR SDRAM when necessary, as shown by the data probe in Fig. 5.

To conduct data analysis and treatment, the PCI bus was chosen as the data bus in this design to communicate between the collecting module and host computer. The system mainly collects transient spectrum information. The data volume is huge, but continuous collection is not necessary. Thus, DDR SDRAM with sufficient volume and high-speed output channel is needed to transmit collected data through PCI. Therefore, the stable and dedicated PCI interface chip PCI9054 (PLX Technology Inc.) was elected to be the bus control unit to communicate with the host computer. This chip fits the PCI2.2 bus standard and supports the low cost subordinate adapter; its clock is 0−33 MHz. The theoretical data transmission rate can achieve 132 Mb/s (60 Mb/s in practice). In this design, the PCI9054 was set in the slave mode, and FPGA acted as the main controller to control the data transmission. There are three bus operating modes for PCI9054: M mode, C mode, and J mode. Among them, the C mode can connect seamlessly with the Intel i960 series high-performance microprocessor and can fulfill most of the practical application demands. Furthermore, its time sequential routine of the local bus operation is the simplest; its logic control and development are relatively easy. Consequently, the C mode is adopted in this design. Figure 6 presents the PCI peripheral interface circuit.

Data are accessed and processed by a special software using a computer. According to the theory of multispectral thermometry, the emissivity function and the real temperature can be obtained using the regression method if the illumination intensity of several wavelengths is the same at the same temperature[10]. The Delphi language is utilized to write the data processing software used to fit the illumination intensity of several wavelengths.

When the spectral dispersion is uniform, the wavelength is assumed to be linear with the location of the CCD pixel[11]. The relationship is expressed by

$$\lambda(x) = ax + b,$$

where x is the pixel location; a and b are constants. According to the equation, two light sources with a known single-wavelength are necessary in the calibration. In the experiment, the characteristic spectral lines of a mercury lamp are used for calibration. After the calibration, the detonation light radiates into the optical system after the explosion. The synchronous photosensitive trigger signal is generated at the same time under the irradiation of the blast waves. After a delay of 30 ns, the acquisition begins to work simultaneously. After acquisition and storage, the host computer reads out the gathered data. Using MATLAB to visualize the data, the curve of spectral intensity is obtained.

In the experiment, the transient spectrum acquisition is applied in one process of detonation. Information on the continuous spectrum radiation in the visible region is acquired and transmitted to the DDR SDRAM. The host computer reads out the data and completes the fitting calculations, through which the transient spectral information of four different times in a detonation is obtained. The curves can be compared with each other after the processing of normalization. The spectrum curves are acquired at 0, 26.8, 53.6 and 107.2 μs, respectively, as shown in Fig. 7.

In conclusion, the design scheme of high-speed spectrum acquisition and storage in this letter is practicable and reliable. The entire controls in the system are realized by some controller modules in FPGA, thus improving the low transmission rate in the general transport system. The temporal resolution of this system depends on the CCD's resolution and is approximately 13.6 μs. The spectral resolution of dispersive spectrometers has a range between a few tenths of a nanometer and 2 nm. In this letter, the spectral range measures 450−800 nm, and theoretically, the spectral resolution can reach about 0.7 nm. Thus, the spectral resolution of the system is not more than 2 nm. This system provides a noval idea in

acquiring and analyzing high-speed spectral information in detonation. Thus, employing AD and gaining higher accuracy is achieved improving the speed and accuracy of this system.

References

1. G. Li, Q. X. Li, L. Lin, X. X. Li, Y. Wang, and Y. L. Liu, Spectrosc. Anal. (in Chinese) **26,** 2177 (2006).
2. Y. L. Bai, K. H. Ren, X. Ou-Yang, F. T. He, W. H. Zou, and B. Y. Xu, Acta Photon. Sin. (in Chinese) **32,** 868 (2003).
3. G. Li, Y. Wang, H. L. Li, and Y. L. Liu, Spectrosc. Spect. Anal. (in Chinese) **27,** 1905 (2007).
4. S. T. Chen, Proc. SPIE **7384,** 73840P (2009).
5. X. Ch. Cai and L. P. Zhai, Proc. SPIE **7283,** 72831F (2009).
6. L. Yan, C. Y. Lei, G. Zhao, S. R. Lee, and K. M. Bae, in *Proceedings of the IEEE International Conference on Industrial Informatics* 1257 (2008).
7. Y. M. Wang and G. Sh. Xu, in *Proceeding of the Ninth ICEMI* 4-500 (2009).
8. D. G. Zhang and M. Li, Mod. Electron. Tech. (in Chinese) **16,** 61 (2007).
9. J. G. Pan, P. W. Que, and H. M. Lei, Electron. Measurement Technol. (in Chinese) **31,** 9 (2008).
10. J. Li, Q. C. Pang, K. H. Ren, and W. D. Peng, Acta Photon. Sin. (in Chinese) **29,** 937 (2000).
11. B. Wang, Y. L. Bai, X. Ou-Yang, B. Y. Liu, X. H. Bai, and J. P. Zhao, Acta Photon. Sin. (in Chinese) **39,** 441 (2010).