All-digital pulse generator for gradually modulated semiconductor laser

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An all-digital design method consisting of a laser drive circuit for gradually modulating the frequency, pulse width, and amplitude of the output of semiconductor laser is demonstrated. Field programmable gate arrays (FPGAs) and accurate delaying chip are used to generate the pulse. The repetition rate and pulse width of the laser pulse gradually adjust from 1 to 10 kHz and 700 ps to 3 ns, respectively. Furthermore, the time of the rising and falling edges for the laser pulse is less than 800 ps.

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The laser diode (LD) has been widely used in laser communications, laser radar, high-speed photography, solid-state lasers, and laser ranging applications, as well as in other areas because of its small size, high efficiency, long life, low cost, *etc.* At present, the demand for gradually adjustable nanosecond pulse sources has become more urgent.

Producing pulses with transistors is a general method. A good pulse shape can be obtained using avalanche photoelectric diode (APD) as a switch; however, the pulse width and the peak current are very difficult to adjust continuously. Moreover, APD requires high voltage to drive, which may generate crosstalk on high-frequency signals[1−3]. Power metallic oxide semiconductor field effecttransistor (MOSFET) is a device whose current is controlled by voltage, therefore, it is convenient to adjust the repetition frequency, pulse width, and peak current continuously. However, it is difficult to attain a pulse width of around 20 ns[4].

In this letter, the pulses are generated by a method used in ultra-wideband (UWB) pulse generators in radar systems. By using this method, real-time gradual and accurate control of pulse width, repetition rate, threshold current, and peak current is realized. The time of the rising and falling edges is less than 800 ps.

The aim of this study is to attain faster rising (falling) edge and better shape of the laser pulses. The design generate electronic pulses by low-voltage differential signaling (LVDS). LVDS can be easily generated by field programmable gate arrays (FPGAs). The clock signals divided by FPGA are utilized to generate two-way square waves with the same duty cycle and adjustable frequency, after which two-way square waves are enabled through a set of precise delay chips (precise delay chips[5]). It is assumed that the square waves at the first path delay A ns, and that the second path delay $A + B$ ns. The two square waves conduct an exclusive-OR operation in FPGA. A pulse with a width of B ns is generated, and the pulse is defined in the form of LVDS. The circuits of pulse generation are shown in Fig. 1.

In the design, square waves with adjustable frequencies were generated by FPGA, and the clock was used with a 24 MHz crystal. The requested repetition frequency of the low-power semiconductor laser was set at 1–10 kHz, so the frequency division at $48000/n$ (n=1, 2,$\cdots$,10) of the clock signals became a viable option. Suppose that the pulse repetition of 4-kHz is requested, the clock signals should be 12000 (n=4) frequency-divided to generate the two-way frequency of 2 kHz and 50% duty cycle square waves. Due to precise delaying and exclusive-OR operation for two-way delayed square waves, we can obtain pulses with 4-kHz repetition frequency. In the same way, given that the maximum of n is 10, the repetition frequency of the pulses can be controlled by taking four pins of FPGA and with decoding circuit.

Given that the pulses were generated by a two-way delay and exclusive-OR operation, the pulse width can be changed by fixing the digital amount of one way and adjusting the digital amount of the other way. For example, if one way is delayed A ns and we need a pulse with width of C ns, the other way should be delayed $A + C$ ns. Using the same principle for adjusting the repetition frequency of the pulses, we could control digitally the width of pulses with the decoding circuits and precise delaying chips.

To obtain faster edge in order to achieve a pulse width of 1 ns, LVDS signal was chosen to transmit the pulse

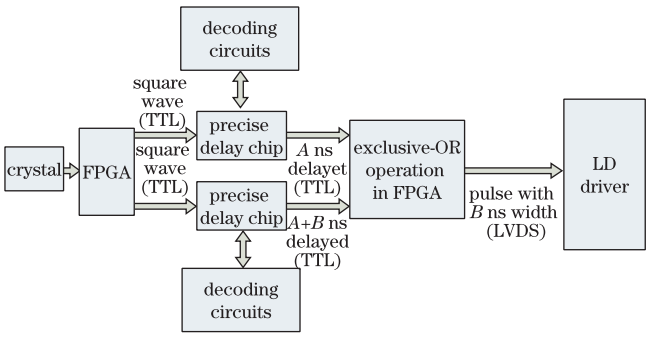

Fig. 1. Structure of the laser driver circuits.

signal. Complex programmable logic device (CPLD) cannot generate LVDS signal; hence, the TTL-LVDS chip

should be used. However, the TTL-LVDS chip is usually not fast enough and the set up and hold times are usually more than 1 ns. Therefore, FPGA was used in this work to generate the LVDS pulse signal. Although the internal resources are section-interconnected and the delay time is unpredictable, experiments have shown that the rising and falling edges do not have much dither.

LMH6526 is a LD driver used in combined DVD/CD recordable and rewritable systems. The LD driver can amplify the current of the pulses effectively and produce a threshold current. It is equivalent to the LD reduces the threshold current of the semiconductor laser and converts the electrical pulses into the light pulses more efficiently. The maximum output current can reach 100 mA. At the same time, the threshold current and the current of the pulses can be accurately real-time controlled by the chip pins with D/A and decoding circuits.

Electrical pulses generated in the experiment are shown in Fig. 2. Lecroy8600A oscilloscope was used to observe the pulse width. Gradually modulated electrical pulses with widths from 800 ps to 50 ns and pulse interval of 500 ps are selected (Figs. (2(a)–(e)). Figure 2(f) shows an electrical pulse adjusted to 50 ns. Compared with the APD circuit, the width of the pulses generated by this design can be adjusted accurately and gradually. The pulse width is narrower than the one generated by Power MOSFET. The amplitude of the pulse is 2 V. The time of the rising edge is less than 650 ps, and the time of the falling edge is less than 700 ps.

Time-domain laser pulses can be obtained by triggering the semiconductor laser with electrical pulses. Figure 2(a) shows gradually adjusted time-domain laser pulses with a pulse width of 800 ps. Compared with Power MOSFET, our method can generate very narrow pulses.

Figure 3 shows that the maximum output of the laser pulses is gradually modulated in 90–200 mV range, which

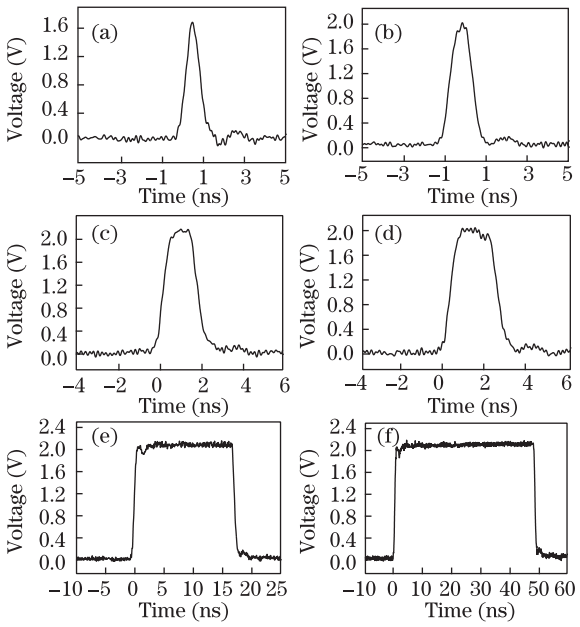

Fig. 2. Results of gradually adjusting the width of the electrical pulses to (a) 800 ps; (b) 1.2 ns; (c) 1.7 ns; (d) 2.2 ns; (e) 17 ns; (f) 50 ns.

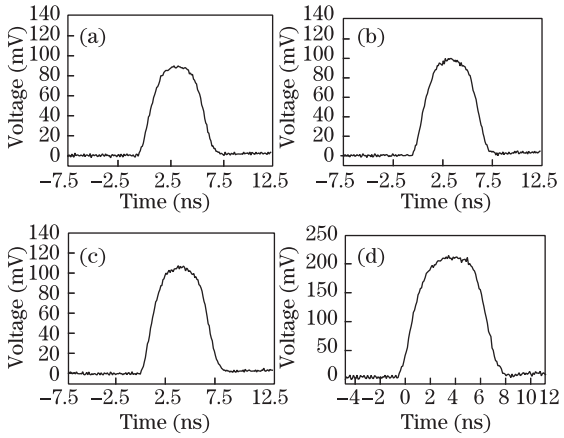

Fig. 3. Results of gradually adjusting the peak of the laser pulses to (a) 90 mV; (b) 100 mV; (c) 110 mV; (d) 200 mV.

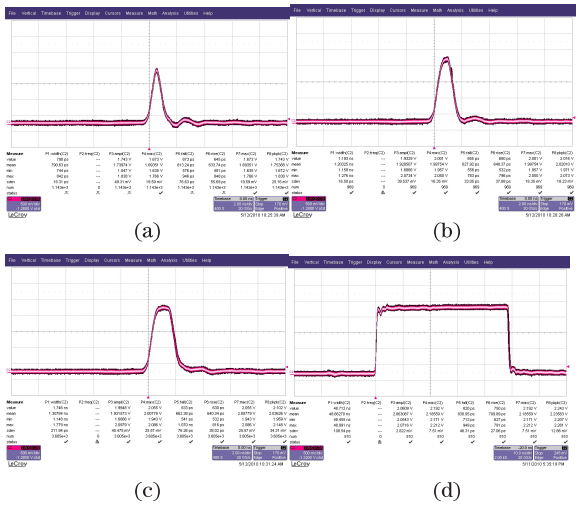

Fig. 4. Dither of continuously adjusting pulses at each width. (a) 800 ps; (b) 1.2 ns; (c) 1.7 ns; (d) 50 ns.

could not be continuously adjusted in the APD circuit.

The dither of the pulses at each width is shown in Fig. 4. Experiments showed that pulses at each width do not have much dither.

As discussed in this design, the pulses generated by the drive circuit that use FPGA can accurately delay chips, high-speed exclusive-OR gate, and LD driver. Moreover, they have the advantages of accurate and continuous regulation, and can be successfully applied to directly modulate semiconductor lasers.

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