Epitaxial growth of low dislocation Ge thin films on Si (001) substrates using a Si-Ge intermediate layer

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Received December 16, 2009

Pure Ge is grown on Si substrate to control the release of the strain in the heterostructure, which is due to the 4.2% lattice misfit between Ge and Si. In this letter, an innovative approach of multi-buffer layers is proposed for the epitaxial growth of high quality Ge thin films on Si (001) substrates in a molecular beam epitaxy system. The multi-buffer layers, including the low temperature Ge seed layer and the Si-Ge alloy intermediate layer fabricated under different temperatures, serve as defect gathering and annihilating sites to reduce the dislocation density in the top layers. The result reveals that the total thickness of the whole structure is less than 400 nm, with a low threading dislocation density of less than 5×10^5 cm^{-2} in the top layer and a root mean square surface roughness of 1.5 nm.

OCIS codes: 310.1860, 310.6845, 310.6870.
doi: 10.3788/COL201008S1.0091.

High quality Ge and Si-Ge alloy has widely been the concern in thin film technology since the late 1980s. Ge has been used as an effective sensitive material in infrared detection devices because it has higher carrier mobility and smaller band gap than Si. This gives Ge better absorption in the wavelength range from 1.3 to 1.5 μm[1−3]. A large lattice mismatch between Ge and Si may introduce a large number of misfit dislocations (10^{10}—10^{12} cm^{-2}) into the heterostructure when directly growing Ge on Si substrates, which may as well inhibit the carrier mobility and lead to a rather big leakage current in the devices[4]. The performance of the device could also be affected by the rough surface of the Ge thin film caused by its stress release.

Accordingly, the earliest solution to this problem is the introduction of a Si-Ge alloy buffer layer, which has a graded composition, into the Ge film and Si substrate[5−7]. The Ge content can increase by 10% per micron, such that the threading dislocation density could be decreased to 2×10^6 cm^{-2}. The system retains its characteristic of large thickness and rough surface. This process can be improved by using As, Sb, Te, and other elements as a surfactant to inhibit the three-dimensional (3D) growing mode of the Ge film and to decrease the surface roughness[7−9]. Alternatively, chemical-mechanical polishing can be employed to improve the surface morphology[6]. A low temperature (LT) buffer layer is also used to grow high quality Ge and Si-Ge thin films[10,11]. This can serve as a trap center for low energy defects to inhibit the climbing of the threading dislocations in the upper films through the intentional introduction of a large quantity of point defects[12]. Recently, the technique of Ge seed layer (SLs) coating has been widely used[13−15]. The Ge or Si-Ge films are grown in high temperature (HT) after preparing an extremely thin (10–30 nm) Ge film in LT. This can effectively decrease the roughness of the surface of the

system. Lee *et al.* used a Si intermediate layer to cut off the threading dislocations in the Si-Ge alloy film to get Si-Ge thin films with minimal dislocations[16]. This paper proposes a new structure fabricated by combining a LT Ge seed layer and a higher temperature for the pure Ge layer, with the incorporation of a Si intermediate layer to decrease the threading dislocation density and the surface roughness.

All the samples investigated in this work were grown on 2-inch p-type Si (001) substrates (resistivity = 1–5 Ω·cm). All the Si wafers were pre-treated by RCA cleaning before the deposition. A molecular beam epitaxy (MBE) system was used, equipped with a reflection high energy electron diffraction (RHEED) to monitor the situation of the samples. Si and Ge materials were grown by electron gun and Knudson furnace, respectively, at a growing pressure of 5×10^{-7} Pa. Prior to the growth of Ge films, the Si (001) substrates were annealed at 1000 °C for 30 min and a 100-nm-thick Si buffer layer was grown at 700 °C to further improve the surface. After the deposition of the Si-Ge structures, characterization was performed using the RHEED patterns, scanning electron microscopy (SEM), and atomic force microscopy (AFM). The threading dislocation density was obtained by calculating the etch pit densities (EPDs) from the wet chemical etch. The etchant was a Ce^{IV} etchant with a concentration of 0.1 mol/L[17].

Three different structures were prepared for comparison. As illustrated in Fig. 1, sample 1 comprises a HT 500 °C Ge film on Si, and sample 2 comprises a LT 300 °C Ge buffer layer before the HT Ge film. The temperature for the fabrication of sample 3 increases as the layers are deposited on to the pure Ge films. There is a Si$_{0.3}$Ge$_{0.7}$ alloy intermediate layer. The thicknesses of these structures were not large considering the limitation of the growth velocity of the MBE system.

The RHEED patterns of the three structures are shown
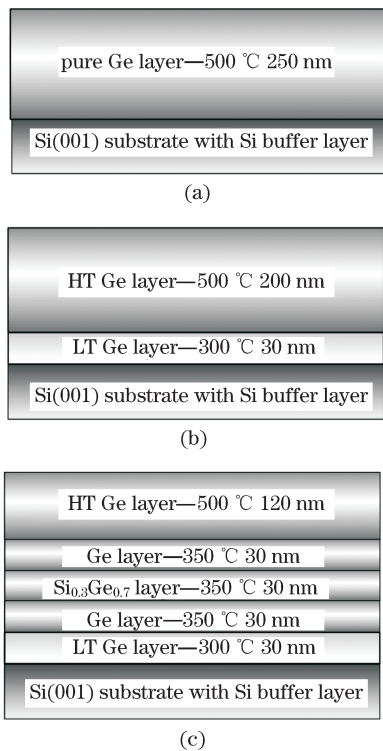
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Fig. 1. Si-Ge films structures. (a) Sample 1, (b) sample 2, and (c) sample 3.
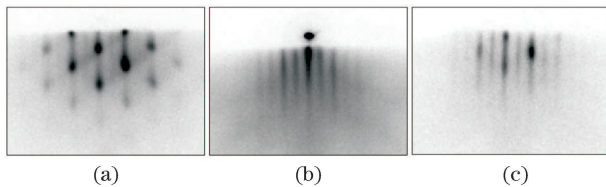
Fig. 2. RHEED patterns from the surfaces of (a) sample 1, (b) sample 2, and (c) sample 3.
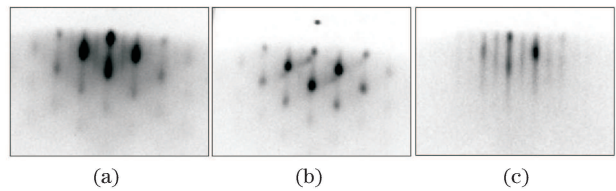

Fig. 3. Evolution of RHEED patterns during the growth of sample 3 (a) after the LT Ge layer, (b) after the intermediated Si-Ge layer, and (c) after the final HT Ge layer.
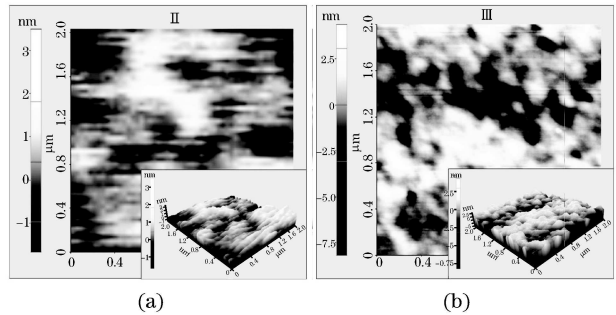

Fig. 4. AFM results of the surface for (a) sample 2 and (b) sample 3 with embedded 3D figures.
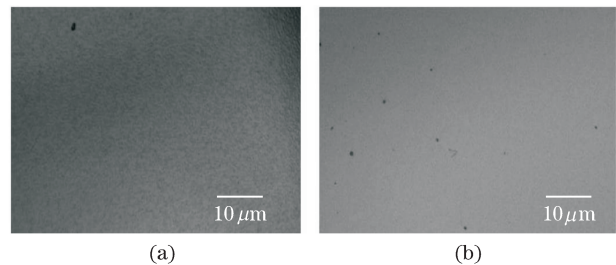

Fig. 5. EPD results of the surface for (a) sample 2 and (b) sample 3.

in Fig. 2. RHEED is a convenient tool for in *situ* monitoring. The glancing incidence of the electron beam makes it sensitive to the surface, and the RHEED patterns directly correspond to the reciprocal space of the crystal. The surface status can be estimated from the pattern, such as spot distribution on the rough single-crystal surface and streaks on a flat surface[18]. From the RHEED patterns, it can be seen that the linearity in Figs. 2(b) and (c) is much greater than that in Fig. 2(a), so samples 2 and 3 have greatly improved surfaces than sample 1. Also, from the evolution of the RHEED pattern of sample 3 (see Fig. 3), the surface roughness grows worse after the alloy intermediate layer.

A degeneration of the surface roughness is also seen for the sample 3 compared with sample 2 (Fig. 2). More details of this are available from the AFM results. As shown in Fig. 4, sample 2 has a better surface, with a root mean square (RMS) roughness of 0.8 nm in the 2 × 2 (μm) limited area. Sample 3 has a roughness of 1.5 nm.

Another important parameter is dislocation density. A selective etching process for defects based on chemicals is a simple and fast way to evaluate the structure perfection of the crystal. The threading dislocation density

is estimated by calculating the EPDs. From the EPD test results (Fig. 5), sample 3 can be seen to have greatly decreased dislocation density from 10^7 to 10^5 cm^{-2}.

A comparison of the samples shows that the LT Ge seed layer could effectively relax the strain from the Si-Ge interface. To some extent, it also inhibits the stretch of dislocation from the Si-Ge interface. Moreover, the alloy intermediate layer could serve as defect gathering and annihilation sites, but it will increase the surface roughness of whole system. This is because that the lattice misfit between that the alloy and pure Ge films will produce more strain in the system.

In conclusion, high quality Ge thin films are fabricated on the Si (001) substrate using a LT buffer layer and Ge-Si alloy intermediate layer. The surface roughness of the Ge film is around 1.5 nm and the threading dislocation density reaches 5×10^5 cm^{-2}. The whole system has a small thickness of less than 400 nm.

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