

Non-feedback precoder for optical DQPSK modulation

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A novel non-feedback precoder circuit for high-speed parallel optical differential quadrature phase shift keying (DQPSK) modulation is proposed. The alternative control signal is introduced in replacement of the conventional feedback one, which eliminates the speed limitation due to the electronic propagation delay. The proposed precoder consists of four differential encoders, an exclusive OR gate, a cross switch, and delay lines. It is demonstrated by a true pseudo random bit sequence (PRBS) transmission at 20 Gb/s.

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Differential quadrature phase shift keying (DQPSK) is considered one of the most promising modulation formats in the next generation high speed optical transmission for its doubled spectral efficiency, enhanced chromatic dispersion (CD) and polarization mode dispersion tolerance^[1,2]. In a DQPSK transmitter, a precoder is indispensable to provide a direct mapping between the input data stream and the modulator driving signal. Conventionally, the precoder outputs are fed back to complete the logic decision^[3], which creates a bottleneck when the signal rate exceeds gigabit per second due to the electrical propagation delay of the feedback path. Therefore, due to the lack of a feasible precoding solution, reported transmission experiments use pre-calculated data pattern in either the transmitter or the receiver^[4,5].

One approach to relax the delay restriction is to multiplex a set of low speed precoder in parallel. A 107-Gb/s pseudo random bit sequence (PRBS) with the length of $2^{23}-1$ is transmitted by incorporating ten 10.7-Gb/s tributaries^[6]. A parallelization scheme using a parallel prefix network is also proposed, and a 20-Gb/s PRBS transmission is demonstrated by a 128-channel expansion with each channel operating at 78 Msymbol/s^[7].

Another method to overcome the speed limitation is to construct an all-forward precoder for a serial DQPSK transmitter^[8]. However, studies indicate that serial modulation suffers from less CD tolerance and nonlinearity tolerance than those of the parallel modulation^[9].

In this letter, we present a novel non-feedback precoding scheme for parallel DQPSK modulation. With two additional differential encoders, an all-forward constructed control signal is introduced for the conventional feedback one by the logic combination of the input signals, eliminating the speed bottleneck due to the feedback path. We demonstrate the concept by a true PRBS transmission at 20 Gb/s with various data lengths. The precoder is implemented with commercially available standard logic integrated circuits (ICs). It can be directly upgraded with higher speed logic components.

The optical DQPSK precoding logic^[10] is

$$\begin{aligned} I_n &= \overline{(I_{n-1} \oplus Q_{n-1})} (I_{n-1} \oplus u_n) \\ &\quad + (I_{n-1} \oplus Q_{n-1}) (I_{n-1} \oplus v_n), \\ Q_n &= \overline{(I_{n-1} \oplus Q_{n-1})} (Q_{n-1} \oplus v_n) \\ &\quad + (I_{n-1} \oplus Q_{n-1}) (Q_{n-1} \oplus u_n), \end{aligned} \quad (1)$$

where I_n and Q_n denote the driving signals of the in-phase and the quadrature-phase components, respectively; I_{n-1} and Q_{n-1} are the 1-bit delayed version of I_n and Q_n , respectively; u_n and v_n indicate the two input data streams of the precoder; the symbol \oplus represents the exclusive OR (XOR) calculation.

Although the precoder is usually implemented according to the sum-of-product equation form in the prior arts^[5], direct carrying out is feasible by incorporating differential encoders, a cross switch, and an XOR gate, as

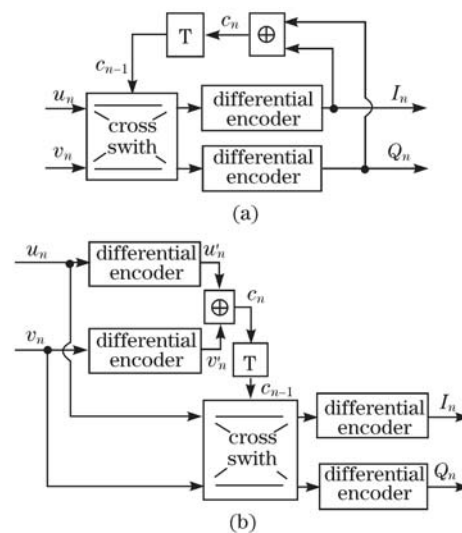


Fig. 1. Block diagram of (a) direct implemented precoder scheme with a feedback control, and (b) proposed non-feedback precoder for optical DQPSK modulation.

shown in Fig. 1(a). Assume $c_{n-1} = (I_{n-1} \oplus Q_{n-1})$ is the control signal of the cross switch which determines the inputs of the two following differential encoders. When c_n is logic low, I_n is the differential encoder output corresponding to the input of u_n , while Q_n is that of v_n ; when c_n is logic high, the two inputs of differential encoders are exchanged. The outputs of the cross switch are differentially encoded separately before the precoder outputs are given out.

To ensure the correct logic function, the overall propagation delay of the loop back path ought to be equal to the data time interval, including several logic gates and their interconnections, which can hardly be achieved in high speed optical transmission.

Due to the commutative and associative characteristic of XOR operation, the control signal c_n remains the same whether the cross switch output changes or not. Therefore we introduce an alternative of the control signal, as shown in Fig. 1(b). Each of the two data inputs is equally divided into two identical streams, respectively, one to implement the control signal and the other to be precoded. In the control path, each stream is encoded by a differential encoder. The differential encoder can be forward constructed by an AND gate and the toggle flip-flop^[11]. The encoded streams u'_n and v'_n , are fed into an XOR gate. After a 1-bit delay, the output of the XOR gate drives the cross switch as the control signal. The coding path is exactly the same as the conventional scheme, with two data streams connected to the two inputs of the cross switch. Outputs of the cross switch are differentially encoded separately before the precoded signal is given out.

In the conventional scheme, derived from Eq. (1), the logic expression of the control signal c_n is

$$c_n = I_n \oplus Q_n = u_n \oplus v_n \oplus I_{n-1} \oplus Q_{n-1} = (u_n \oplus I_{n-1}) \oplus (v_n \oplus Q_{n-1}). \quad (2)$$

The logic expression of c_n in our proposed scheme is

$$c_n = (u'_n \oplus v'_n) = (u_n \oplus u'_{n-1}) \oplus (v_n \oplus v'_{n-1}), \quad (3)$$

where u'_n and v'_n denote the differential encoder output of u_n and v_n , respectively, while the subscript $(n-1)$ indicates the 1-bit delayed version.

We implemented the precoder by standard logic ICs and the printed circuit board (PCB), as shown in Fig. 2. Radio frequency (RF) cables are employed for interconnection and delay length control. A randomly selected sequence pattern measurement of precoder inputs, outputs with the corresponding modulation carrier phase, and demodulation phase shift are plotted in Fig. 3. The input is PRBS (2^7-1) and the measured data length

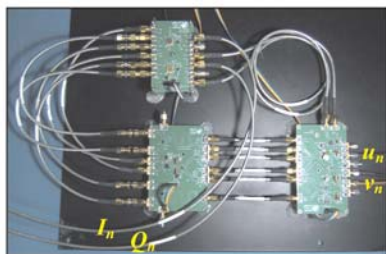


Fig. 2. Prototype of the proposed precoder.

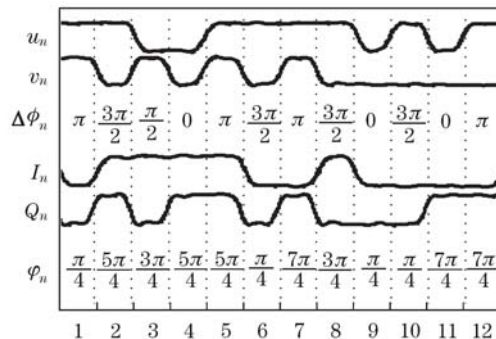


Fig. 3. Measured waveforms of precoder inputs (u_n , v_n), the corresponding demodulation phase shift ($\Delta\phi_n$), precoder outputs (I_n , Q_n), and modulation carrier phase (ϕ_n).

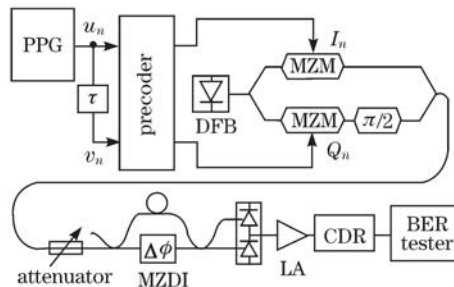


Fig. 4. Experimental setup for the proposed precoder.

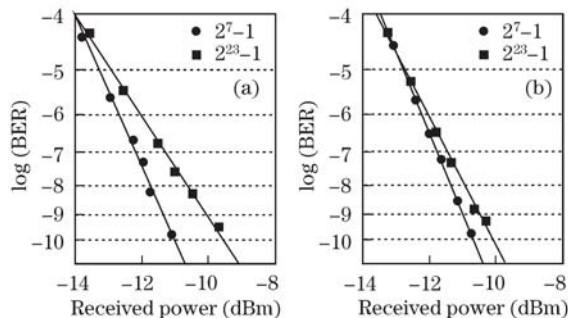


Fig. 5. Measured BER performance with PRBS (2^7-1) and PRBS ($2^{23}-1$) for (a) u_n and (b) v_n .

is 12. The precoding logic function can be verified by examining each bit of the inputs and their corresponding outputs, shown in the carrier phase relationship in

$$\phi_{n+1} = \phi_n + \Delta\phi_n, \quad (4)$$

where ϕ_n denotes the modulation carrier phase and $\Delta\phi_n$ indicates the phase shift.

The precoder is demonstrated in the optical DQPSK transmission system illustrated in Fig. 4. A pulse pattern generator (PPG) generates a PRBS with the data rate of 10.709 Gb/s. The PRBS is split and fed to the precoder as u_n and v_n , respectively. A delay line which delays the data for 2.24 ns is added before v_n for de-correlation. The optical carrier is provided by a distributed feedback (DFB) laser, operating at 1552.788 nm, and modulated by a dual parallel Mach-Zender modulator (MZM). Each MZM is biased at the transmission null and driven with the precoder outputs I_n and Q_n , respectively, with the peak-to-peak amplitude of $2V_\pi$. An additional $\frac{\pi}{2}$ phase shift is added to the Q_n branch. The DQPSK demodulator incorporates a Mach-Zender delay interferometer

(MZDI). The delay in the MZDI upper arm equals the data time interval and the phase shift is tuned to $\pm\pi/4$ for either u_n or v_n tributary. The demodulated data is received by a 50-GHz balanced photodetector and regenerated by a limiting amplifier (LA) and a clock data recovery (CDR), respectively. To evaluate the system performance, an optical attenuator is added before the demodulator, and the receiver sensitivity is measured.

We measured the bit error rate (BER) performance with PRBS (2^7-1) and PRBS ($2^{23}-1$) for both tributaries, as plotted in Fig. 5. The receiver sensitivity is about -10 dBm at 10^{-10} BER because the employed 50-GHz balanced photodetector exhibits lower optical responsivity and higher noise bandwidth. The received power degradation from PRBS ($2^{23}-1$) to PRBS (2^7-1) is approximately 1.5 dB for u_n and 0.6 dB for v_n . This mainly results from the low pass characteristic of precoder PCB and the instability of MZDI.

In conclusion, a novel non-feedback optical DQPSK precoder is proposed. The conventional feedback control signal is replaced by an all-forward constructed one, with two additional differential encoders. The precoder is implemented with standard logic ICs and demonstrated by true PRBS transmission with different data lengths.

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