Configuration of an optical waveguide interconnect mesh network based on EOPCB

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An optical waveguide interconnect mesh network scheme for parallel multiprocessor systems based on an electro-optical printed circuit board (EOPCB) with multimode polymer waveguide is proposed. The system consists of 2×2 processor element chips interconnected in a mesh network configuration. An additional layer with optical waveguide structure is embedded in a conventional printed circuit board to construct the EOPCB. Vertical cavity surface emitting laser (VCSEL)/positive intrinsic-negative (PIN) arrays are applied as the optical transmitters/receivers. Three 1×12 VCSEL/PIN parallel optical transmitting/receiving modules are used to provide 32 input/output optical channels required by the 2×2 chip-to-chip optical mesh interconnect system. The data rate in each optical channel is 3.125 Gbps and thus 10 Gbps parallel optical interconnect link for each direction of a chip is obtained. The optical signals from a processor element chip can be transmitted to another chip through optical waveguide interconnect embedded in the board. Thus the optical interconnect mesh network for parallel multiprocessor system can be implemented.

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Conventional electronic systems become inadequate for the manipulation and processing of large data equipments. The future multiprocessor systems require an innovative interconnect technology substituting for the conventional electronic one which is the bottleneck of the current systems. Optical interconnect is expected to be the technology due to its excellent potential. Its advantages include high speed, wide bandwidth, free of electromagnetic interference, and signal reflection[1,2]. Chip-to-chip optical interconnect on a printed circuit board (PCB) board is an important technique to improve the data rate and bandwidth of signal transmission between chips[3−11]. The mesh network is one of the most popular topology for parallel processing. It can perform four typical connections: (a) left-shift connection; (b) right-shift connection; (c) under-shift connection; (d) upper-shift connection[12−15]. An optical waveguide interconnect mesh network scheme for parallel multiprocessor systems based on electro-optical printed circuit board (EOPCB) with multimode polymer waveguide is proposed in this letter. The system consists of 2×2 processor element chips interconnected in a mesh network configuration. Four parallel optical interconnect channels are arranged in each of the four directions of a chip. Two channels are used for optical transmitting with E/O conversion, and the other two channels for optical receiving with O/E conversion. Thus there are totally eight transmitting and eight receiving channels for one chip. So 32 transmitting and 32 receiving channels are required for the 2×2 chip-to-chip optical mesh interconnect configuration. The switching chip is employed for routing control of the mesh interconnect. An additional layer with optical waveguide is embedded in a conventional PCB to construct the electro-optical printed circuit board (EOPCB). Vertical cavity surface emitting laser (VCSEL) arrays are used as the optical transmitters and positive intrinsic-negative (PIN) photodiode arrays are used as the optical receivers. The optical signals from one processor element chip can be transmitted to another chip through optical waveguide interconnect embedded in the board. Thus the optical interconnect mesh network for parallel multiprocessor system can be realized.

The mesh interconnect network is also called four nearest neighbor interconnect network. The scheme of a 4×4 mesh interconnect network topology for $N = 16$ is shown in Fig. 1. The labels 0, 1,. . . , 15 are the addresses of the processor elements (PEs).

The interconnect functions of the mesh network can be described as

$$R_{+1}(i) = (i+1) \bmod N \quad \text{(right-shift connection)}, \quad (1)$$

$$R_{-1}(i) = (i-1) \bmod N \quad \text{(left-shift connection)}, \quad (2)$$

$$R_{+r}(i) = (i+r) \bmod N \quad \text{(under-shift connection)}, \quad (3)$$

$$R_{-r}(i) = (i-r) \bmod N \quad \text{(upper-shift connection)}, \quad (4)$$

where $r = \sqrt{N}$, $0 \le i \le N-1$, i is the source address of the PE, and R is the destination address of the PE.

The four direction interconnects for the mesh network

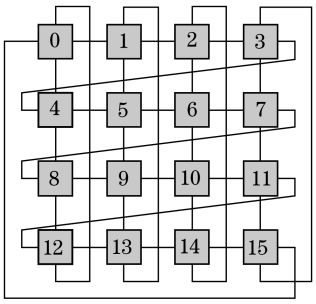


Fig. 1. Schematic of the mesh interconnect network topology

for $N = 16$.

with N=16 are shown in Fig. 2. Each PE can only connect to the four nearest neighboring PEs. In order to implement the optical mesh interconnect, the structure of the EOPCB is proposed, as shown in Figs. 3(a) and (b)[15]. An additional optical layer with multimode polymer waveguide is imbedded in a conventional multilayer PCB to provide optical transmission paths. VCSEL/PIN transceiver arrays are used for optical signal parallel transmission between chips on the PCB. Each PE chip is accompanied with a VCSEL array and a PIN array. VCSEL/PIN arrays provide four bi-directional optical communication links to adjacent PE chips on the same PCB: upper-, under-, left-, and right-direction. The VCSEL array with driver integrated circuit (IC) chip and the PIN array with amplifier IC chip are packaged with the PE chips in a non-connectorized ball grid array (BGA) package through the VCSEL/PIN interface circuit boards to form the optical-I/O chip packaging. High speed signals are E/O converted in the BGA optical-I/O chip package and then transmitted to the waveguide layer of the EOPCB. The optoelectronic packages of VCSEL/PIN arrays are surface-mounted on the PCB. VCSEL/PIN arrays are fixed on the heat sinks with the electrode connecting patterns. The VCSEL driver integrated (IC) chip and the PIN amplifier IC chip are bonded with the VCSEL/PIN arrays through the electrode connecting pattern. MT ferrule is a standard interface for optical parallel link[16]. A MT-compatible coupling interface is used for coupling between the VCSEL/PIN arrays on the optoelectronic I/O chips and the waveguide transmission paths on the EOPCB, as shown in Fig. 3(a). Thus the chip-to-chip high speed optical interconnect on the EOPCB can be implemented.

The topological structure of the 2×2 chip-to-chip mesh interconnects on the EOPCB with optical waveguide is shown in Fig. 4. It can perform four typical connections[14]. There are four parallel optical interconnection channels in each of the four directions of one chip. Two channels are used for optical transmitting with E/O conversion, and the other two channels for optical receiving with O/E conversion. There are totally eight transmitting and eight receiving channels for one chip. Thus 32 transmitting and 32 receiving channels are required for the 2×2 chip-to-chip optical mesh interconnect structure. The switching chip is used for routing control of mesh interconnects. The type of the switching chip is VSC3312 which is a 6.5 Gbps 12×12 crosspoint switching chip.

The layout of the optical waveguide layer with VCSEL/

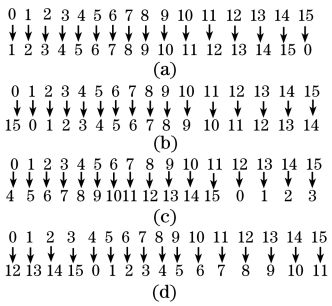


Fig. 2. Four direction interconnects for the mesh network with $N = 16$: (a) right-shift connection; (b) left-shift connection; (c) under-shift connection; (d) upper-shift connection.

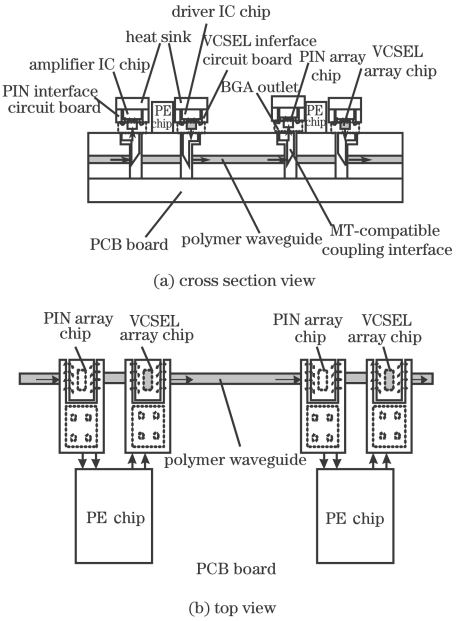


Fig. 3. Structure of the EOPCB with optical waveguide.

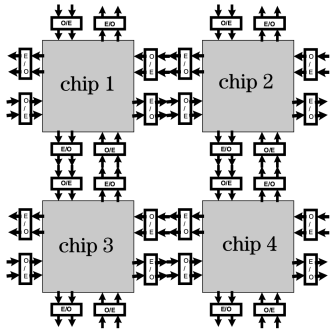


Fig. 4. Topological structure of the 2×2 chip-to-chip mesh interconnects on the EOPCB.

PIN transceiver arrays on the EOPCB is shown in Fig. 5. The system consists of 2×2 processor element chips interconnected in a mesh network configuration. Three 1×12 VCSEL/PIN parallel optical transmitter/receiving modules are used to provide 32 output and 32 input channels required by the 2×2 chip-to-chip mesh interconnect. The other 4 pairs of light transmitting and receiving channels are idle. The data rate of each optical channel is 3.125 Gbps. 10-Gbps parallel optical interconnect link for each direction of a chip can be obtained. The MT-compatible coupling interface is used for coupling between the VCSEL/PIN arrays on the optoelectronic I/O chips and the multimode polymer waveguide transmission paths on the EOPCB. Thus the chip-to-chip high speed optical interconnect on the EOPCB can be obtained.

The right-, left-, under-, and upper-shift connections for chip 1 are also shown in Fig. 5. In order to realize the right-shift connection, the signals must be transmitted from chip 1 to chip 2. The electrical signals from chip 1 are transmitted to input ports 5 and 6 of 1×12 VCSEL transmitter array 1. Thus optical signals are driven and

transmitted into the corresponding channels through the MT-compatible coupling interface. After transmission in the waveguides, the optical signals radiate on the corresponding optical windows of the channels 5 and 6 of the

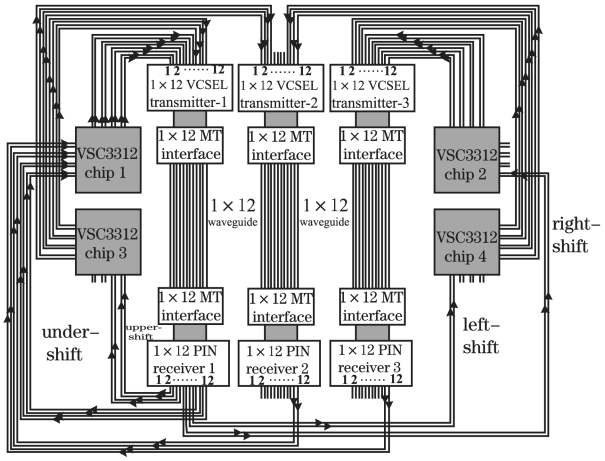
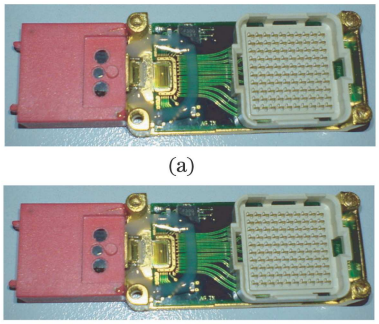


Fig. 5. Layout of the 2×2 chip-to-chip optical waveguide mesh interconnects with VCSEL/PIN transceiver arrays on the EOPCB.



(a)

(b)

Fig. 6. Photos of (a) VCSEL optical transmitting array module and (b) PIN optical receiving array module.

PIN receiver array 1 through another MT-compatible coupling interface. After O/E conversion, the electrical signals are transmitted from channels 5 and 6 of the PIN receiver array 1 to chip 2. Thus right-shift connection from chip 1 to chip 2 is implemented. In the same way, left-shift, under-shift, and upper-shift connections for chip 1 can be implemented according to the topological structure of the 2×2 mesh interconnect. Chip 1 can also receive signals from chips 2, 3, and 4, thus a bi-directional chip-to-chip interconnect is realized.

In order to realize optical transmission between chips on the EOPCB, VCSEL array, and PIN array with wavelength of 850 nm are used as the optical transmitters and optical receivers, respectively. 1×12 parallel VCSEL/PIN array modules with 3.125 Gbps per channel are fabricated. A throughput of 38 Gbps can be obtained with parallel data transmission. Figure 6 shows the optical transmitting module with VCSEL array and the optical receiving module with PIN array . A MT-compatible coupling interface with a 45° endface is used to implement light coupling between the optical transmitter/receiver and the waveguide layer. Figure 7 shows the light coupling interface which can deflect the optical signals by 90°. The VCSEL chip is placed close to the end face of the interface. The channel pitch is 250 μm and the positioning precision is < 0.5 μm, which meets the precision requirements for parallel optical coupling.

A multimode polymer waveguide is used to provide parallel optical transmission channels in the EOPCB. SU-8 photoresist is used to fabricate the waveguide mould with the doctor-blading technique[17]. The pattern of the mould for the waveguide core layer is shown in Fig. 8.

With the SU-8 waveguide mould, we fabricated the waveguide layer embedded in the EOPCB with the Doctor-blading technique, which shows advantage in the fabrication of large-area waveguide layers[13]. Polysiloxane is used as the material of waveguide core and cladding layers. The waveguide cores are fabricated using the Doctor-blading technique by filling the grooves of the SU-8 mould with the core material firstly. Then the core material is thermally cured under 70 °C for 30 min. In order to fabricate the under- and upper-cladding layers, the substrate carriers are made to control the thickness of the cladding layers. FR4 material is used to prepare the substrate carriers. The cladding material is filled in the SU-8 mould with the cured waveguide cores already in it. The substrate carrier is pressde against the SU-8 mould and the cladding layer is cured together with the cores under 70 °C for 30 min, and then the waveguide layers and the carrier are demoulded from the SU-8 mould. Figure 9 shows the micrograph of the waveguide cores. The sectional profile of the waveguide core is measured with the Wyko NT1100 optical profiling system and shown in Fig. 10. The thickness of the waveguide cores is about 50 μm. The FR4 substrate carriers with optical waveguide layers are laminated with the conventional multilayer PCB to construct the EOPCB. The

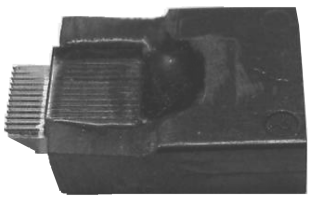


Fig. 7. MT-compatible optical coupling interface with 45° angled endface.

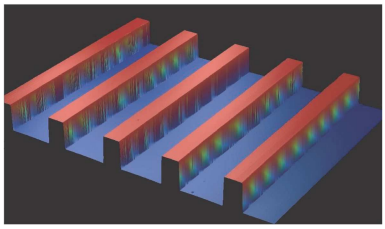


Fig. 8. Pattern of SU-8 mould for waveguide core layer.

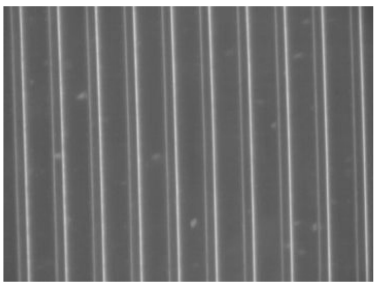


Fig. 9. Micrograph of the waveguide core layer.

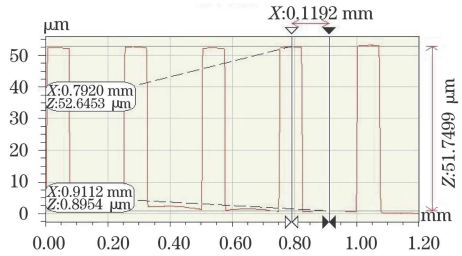


Fig. 10. Sectional profile of the waveguide core layer.

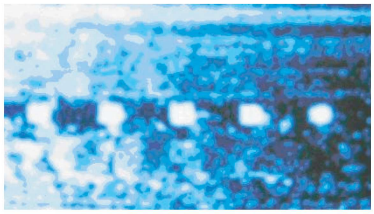


Fig. 11. Sectional view of the EOPCB embedded with FR4 polymer optical waveguide layer.

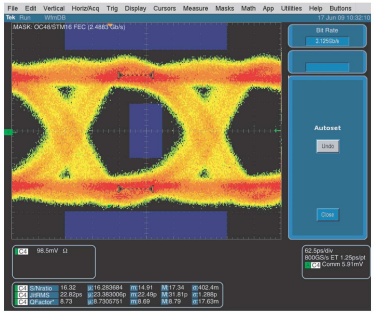


Fig. 12. Eye diagram of 3.125 Gbps per channel.

sectional view of the EOPCB embedded with the FR4 polymer waveguide layer is shown in Fig. 11. The core size of the polymer waveguides is about 70 ×50 (μm). The center-to-center spacing of the adjacent channels is 250 μm. The refractive index of the core and the cladding is 1.43 and 1.41, respectively. The insertion loss is 6.28 dB for a waveguide length of 4 cm.

VCSEL array and PIN array with the wavelength of 850 nm are used as the optical transmitters and optical receivers on the EOPCB, respectively. 1×12 parallel VCSEL/PIN array modules with 3.125 Gbps per channel are fabricated. The eye diagram of 3.125 Gbps per channel is shown in Fig. 12, which is an electrical output of the whole link (signal generator – E/O-module – optical PCB – O/E-module – oscilloscope). The eye was wide open, the signal-to-noise ratio is 16.32, the jit root-mean-square is 22.82 ps, the Q-factor is 8.73, and the bit error rate is 1.3×10^{-12}.

In conclusion, an optical waveguide interconnect mesh network scheme based on the EOPCB is proposed. The system consists of 2×2 chips interconnected in a mesh configuration. The data rate in each optical channel is 3.125 Gbps. 10-Gbps parallel optical interconnect link for each direction of the chip is implemented by two input and two output parallel channels. The optical signals are transmitted from one chip to another one through the optical waveguide layer in the EOPCB. Thus chip-to-chip high-speed optical mesh interconnect on the EOPCB can be realized.

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