# All-optical adder/subtractor based on terahertz optical asymmetric demultiplexer 

Dilip Kumar Gayen ${ }^{1 *}$, Rajat Kumar Pal ${ }^{2}$, and Jitendra Nath Roy ${ }^{3}$<br>${ }^{1}$ Department of Computer Science, College of Engineering and Management, Kolaghat, India<br>${ }^{2}$ Department of Computer Science and Engineering, Calcutta University, Kolkatta-700009, India<br>${ }^{3}$ Department of Physics, College of Engineering and Management, Kolaghat<br>KTPP Township, Midnapur (East), 721171, W.B., India<br>*E-mail: dilipgayen@yahoo.com

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#### Abstract

An all-optical adder/subtractor (A/S) unit with the help of terahertz optical asymmetric demultiplexer (TOAD) is proposed. The all-optical A/S unit with a set of all-optical full-adders and optical exclusiveORs (XORs), can be used to perform a fast central processor unit using optical hardware components. We try to exploit the advantages of TOAD-based optical switch to design an integrated all-optical circuit which can perform binary addition and subtraction. With computer simulation results confirming the described methods, conclusions are given.


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The emergence of increasingly high speed digital optical system and optical processor demands an all-optical adder/subtractor (A/S) unit to perform a set of optical arithmetic micro-operations. All-optical A/S units have many potential applications in optical communication systems and optical computing. Various architectures, algorithms, and logical and arithmetic operations have been proposed in the field of optical/optoelectronic computing and parallel signal processing in last few decades ${ }^{[1-9]}$. Terahertz optical asymmetric demultiplexer (TOAD) based gate has already played significant roles in the field of ultra-fast all-optical information processing ${ }^{[10-14]}$. Sokoloff et al. demonstrated a new device, the TOAD capable of demultiplexing data at $50 \mathrm{~Gb} / \mathrm{s}^{[10]}$. They have also demonstrated demultiplexing of a single channel from a $250-\mathrm{Gb} / \mathrm{s}$ data stream. TOAD exploits the strong, slow optical nonlinearities presented in semiconductor and permits control and signal pulses to be distinguished by polarization or wavelength, and it requires less than 1-pJ switching energy ${ }^{[10]}$. In our earlier paper, we proposed TOAD-based tree architecture for all-optical logic and arithmetic operations ${ }^{[15]}$, alloptical arithmetic unit ${ }^{[16]}$ and number conversion scheme ${ }^{[17]}$. In this letter, we propose a TOAD-based switch to design an integrated all-optical circuit which can perform binary addition and subtraction. With the help of TOAD-based all-optical full-adder and optical exclusive-OR (XOR), we propose an A/S unit which can work in all-optical domain. Simulation of proposed design has also been done with the help of Matlab-6.5.

The TOAD consists of a loop mirror with an additional intraloop $2 \times 2$ (ideally $50: 50$ ) coupler. The loop contains a control pulse (CP) and a nonlinear element (NLE) that is offset from the loop's midpoint by a distance $\Delta x$ as shown in Fig. 1(a) ${ }^{[10]}$. In this letter, we try to take the output from the reflecting mode and transmitting mode of the device.

The output power at port-1 and port-2 can be expressed as ${ }^{[18,19]}$

$$
\begin{align*}
P_{\mathrm{out}}(t)= & \frac{P_{\mathrm{in}}(t)}{4} \cdot\left\{G_{\mathrm{cw}}(t)+G_{\mathrm{ccw}}(t)\right. \\
& \left.\mp 2 \sqrt{G_{\mathrm{cw}}(t) \cdot G_{\mathrm{ccw}}(t)} \cdot \cos (\Delta \varphi)\right\} \tag{1}
\end{align*}
$$

where $G_{\mathrm{cw}}(t)$ and $G_{\mathrm{ccw}}(t)$ are the power gains between cw and ccw pulse, respectively, the phase difference $\Delta \varphi=-\alpha / 2 \cdot \ln \left(G_{\mathrm{cw}} / G_{\mathrm{ccw}}\right)$, and $\alpha$ is the line-width enhancement factor. In the absence of a control signal, the incoming signal enters the fiber loop and passes through the semiconductor optical amplifier (SOA) at different time as they counter-propagate around the loop, experiencing the same unsaturated amplifier gain $G_{0}$, and recombining at the input coupler, i.e., $G_{\mathrm{ccw}}=G_{\mathrm{cw}}$. Then $\Delta \varphi=0$ and expression for $P_{\text {out }, 1}(t)=0$ and $P_{\text {out }, 2}(t)=P_{\text {in }}(t) \cdot G_{0}$. It shows that the data is reflected back towards the source. When a control pulse is injected into the loop, it saturates the SOA and changes its index of refraction. As a result, the two counter-propagation data signals will experience a differential gain saturation profiles, i.e., $G_{\mathrm{ccw}} \neq G_{\mathrm{cw}}$. Therefore they recombine at the input coupler, and then $\Delta \varphi \approx \pi$. The data will exit from the output port-1 and $P_{\mathrm{out}, 2}(t) \approx 0$. A polarization or wavelength filter may be used at the output to reject the control and pass the input pulse. Now it is clear that in the absence of control signal, the incoming pulse exits through the input port of TOAD and reaches the output port-2 as shown in Fig. 1(a). In this case no light is present in the output port-1. But in the presence of control signal, the incoming signal exits through the output port of TOAD and reaches to the output port-1 as shown in Fig. 1(a). In this case no light is present in the output port-2. In the absence of incoming signal, port-1 and port- 2 receive no light as the filter blocks the control

(a)

control signal
(b)

Fig. 1. (a) TOAD-based optical switch; (b) schematic diagram of TOAD-based optical switch.


Fig. 2. Simulated wave form of TOAD-based optical switch.


Fig. 3. All-optical XOR gate. BC: beam combiner; PLS: constant pulse light source.
signal. Schematic block diagram is shown in Fig. 1(b) and the truth table of the operation is given in Table 1.

Table 1. Truth Table of Fig. 1

| Incoming <br> Signal | Control <br> Signal | Output <br> Port-1 | Output <br> Port-2 |
| :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

Simulated wave form for TOAD-based switch is shown in Fig. 2. In this simulation, $\alpha$ is taken as 4 , unsaturated single-pass amplifier gain $G_{0}=10 \mathrm{dBm}$, gain recovery time $\tau_{\mathrm{e}}=100 \mathrm{ps}$, eccentricity of the loop of TOAD $T$ $=50 \mathrm{ps}$, gain saturation time $t_{\mathrm{s}}=40 \mathrm{ps}$, injected control pulse energy $U_{\text {in }}=10 \mathrm{fJ}$, and saturation energy of the SOA $U_{\text {sat }}=200$ fJ. Here we take the incoming pulse power of 1 mW .
The XOR circuit has two inputs (X, Y) and one output (Z). Schematic diagram of TOAD based all-optical XOR is shown in Fig. 3. This circuit uses three TOAD-based optical switches, namely $s_{1}, s_{2}$ and $s_{3}$. Final output (Z) is taken from combining T-3 and T-2 with a beam combiner BC. Let us explain the working principle of XOR as shown in Fig. 3 in detail.
Case 1: $\mathrm{X}=0$ and $\mathrm{Y}=0$
The terminal T-1 only receives the light. Final output is taken from combining T-3 and T-2 with a beam combiner BC . So no light is present in output (Z), i.e., $\mathrm{Z}=0$.

Case 2: $\mathrm{X}=1$ and $\mathrm{Y}=0$
The terminal T-3 only receives the light. So light is present in output ( Z ), i.e., $\mathrm{Z}=1$.
Case 3: $\mathrm{X}=0$ and $\mathrm{Y}=1$
The terminal T-2 only receives the light. So light is present in output ( Z ), i.e., $\mathrm{Z}=1$.
Case 4: $\mathrm{X}=1$ and $\mathrm{Y}=1$
The terminal T-4 only receives the light and no other terminals receive any light. So no light is present in output $(Z)$, i.e., $Z=0$. Here overall transfer function is given by ${ }^{[18]}$

$$
\begin{equation*}
\text { Cascade }(t, \delta)=S W_{1}(t) \times S W_{2}(t-\delta) \tag{2}
\end{equation*}
$$

where $\delta$ is the delay offset time. Here incoming power of TOAD $\mathrm{s}_{2}$ and $\mathrm{s}_{3}$ are $\left[P_{\mathrm{out}, 1}(t)\right]_{\mathrm{s}_{1}}$ and $\left[P_{\mathrm{out}, 2}(t)\right]_{\mathrm{s}_{1}}$, respectively.
The full-adder circuit adds three one-bit binary numbers ( $\mathrm{A}, \mathrm{B}, \mathrm{C}_{\mathrm{in}}$ ) and gives the outputs in two one-bit binary numbers, a sum $(\mathrm{S})$ and a carry $\left(\mathrm{C}_{\text {out }}\right)$. Operational principle of one bit optical full-adder has been explained in Refs. [15] and [16]. Schematic diagram is shown in Fig. 4.

The various circuits used to execute data-processing instructions are usually combined in a single circuit called an arithmetic-logic unit (ALU). A/S is the part of the arithmetic unit. Depending on the mode $A / S$ value it can perform either addition or subtraction. A/S unit with the help of all-optical XOR and alloptical full-adder is explained below. It is to be noted that the output of a TOAD-based switch can be used as the control signal for others provided its intensity is increased suitably through erbium-doped fiber amplifier (EDFA) and the wavelength is changed through


Fig. 4. Optical circuit for 1-bit all-optical full-adder.


Fig. 5. All optical 4-bit A/S unit. $\triangleright:$ EDFA; $\mid:$ WC.
wavelength converter (WC). The optical circuit, as shown in Fig. 5, can perform two different arithmetic operations with two 4 -bit input numbers $\mathrm{A}\left(\mathrm{A}_{3} \mathrm{~A}_{2} \mathrm{~A}_{1} \mathrm{~A}_{0}\right)$ and $\mathrm{B}\left(\mathrm{B}_{3} \mathrm{~B}_{2} \mathrm{~B}_{1} \mathrm{~B}_{0}\right)$. It gives the output $\mathrm{D}\left(\mathrm{D}_{4} \mathrm{D}_{3} \mathrm{D}_{2} \mathrm{D}_{1} \mathrm{D}_{0}\right)$, depending on the value of mode $(\mathrm{A} / \mathrm{S})$. Let us consider an example, where $\mathrm{A}=1100\left(\mathrm{~A}_{3} \mathrm{~A}_{2} \mathrm{~A}_{1} \mathrm{~A}_{0}\right)$ and $\mathrm{B}=1001$ $\left(B_{3} B_{2} B_{1} B_{0}\right)$. The operational principles of two cases are described in details.

Case 1: mode $(\mathrm{A} / \mathrm{S})=0$
The mode $(\mathrm{A} / \mathrm{S})$ is used as one input to XOR and the other input is $B$. As the mode $(A / S)=0$, the one input of the XOR is 0 . According to the operational principle of the XOR, the output will be equal to the value of B. So the XOR-1, XOR-2, XOR-3, and XOR-4 will produce the output equal to the value of $\mathrm{B}_{0}, \mathrm{~B}_{1}, \mathrm{~B}_{2}$, and $\mathrm{B}_{3}$, respectively. Now the output of each XOR is connected to one input (B) of full-adder through wavelength converter and EDFA. So the full-adders FA-1, FA-2, FA-3, and FA-4 receive the value of $B_{0}, B_{1}, B_{2}$, and $B_{3}$ as one input (B), respectively. As $A_{0}$ is directly connected to one input
(A) of the full-adder FA-1, so the input (A) receives the value of $A_{0}$. Similarly, the full-adders FA-2, FA-3, and FA-4 receive the values of $\mathrm{A}_{1}, \mathrm{~A}_{2}$, and $\mathrm{A}_{3}$ as one input (A), respectively. Now in FA-1, the carry in $\mathrm{C}_{\text {in }}$ is 0 . As the mode $(\mathrm{A} / \mathrm{S})=0$, and the other two inputs (i.e., A and $B$ ) receive the values 0 and $1\left(\right.$ as $A_{0}=0$ and $B_{0}=$ 1). According to the operational principle of full-adder, the output $\mathrm{D}_{0}$ takes the value one, i.e., $\mathrm{D}_{0}=1$, and the carry out receives the value zero, i.e., $\mathrm{C}_{\text {out }}=0$. Now the carry out $\mathrm{C}_{\text {out }}$ of full-adder FA-1 is connected to the carry in $\mathrm{C}_{\text {in }}$ of the full-adder FA-2 through wavelength converter and EDFA. In this way, $\mathrm{C}_{\mathrm{in}}$ of full-adder FA-2, FA-3, and FA-4 will be equal to $\mathrm{C}_{\text {out }}$ of the full-adder FA-1, FA-2, and FA-3, respectively. So in FA-2, C $\mathrm{C}_{\mathrm{in}}=$ 0 (as $\mathrm{C}_{\text {out }}$ of the full-adder FA-1 is zero), and the other two inputs ( A and B ) both receive the value 0 (as $\mathrm{A}_{1}=$ 0 and $\mathrm{B}_{1}=0$ ). In this case output $\mathrm{D}_{1}=0$ and $\mathrm{C}_{\text {out }}=$ 0 . Similarly in FA-3, $\mathrm{C}_{\mathrm{in}}=0$, and the other two inputs ( A and B ) receive the values 1 and 0 (as $\mathrm{A}_{2}=1$ and $\mathrm{B}_{2}=0$ ), respectively. Hence $\mathrm{D}_{2}=1$ and $\mathrm{C}_{\text {out }}=0$. Finally in FA-4, $\mathrm{C}_{\mathrm{in}}=0$, and the other two inputs (A and B ) both receive the value of 1 (as $\mathrm{A}_{3}=1$ and $\mathrm{B}_{3}=$ 1), so $\mathrm{D}_{3}=0$ and $\mathrm{C}_{\text {out }}=1$. Here the output $\mathrm{D}_{4}$ takes the value 1 as $\mathrm{C}_{\text {out }}$ is 1 . The final output (D) is 10101 $\left(\mathrm{D}_{4} \mathrm{D}_{3} \mathrm{D}_{2} \mathrm{D}_{1} \mathrm{D}_{0}\right)$ that verifies the addition of two 4 -bit numbers. The simulated wave form is given in Fig. 6.
Case 2: mode $(A / S)=1$
As the mode $(\mathrm{A} / \mathrm{S})=1$, the one input of the XOR is 1 . According to the operational principle of the XOR, the output will be equal to the complement of B (i.e., $\bar{B}$ ). So the XOR-1, XOR-2, XOR-3, and XOR-4 will produce the output equal to the value of $\bar{B} 0, \bar{B} 1, \bar{B} 2$, and $\bar{B} 3$, respectively. Now the output of each XOR is connected to one input (i.e., B) of full-adder through wavelength converter and EDFA. So the full-adders FA-1, FA-2, FA3 , and FA- 4 receive the values of $\bar{B} 0, \bar{B} 1, \bar{B} 2$, and $\bar{B} 3$ as one input (B), respectively. As $\mathrm{A}_{0}$ is directly connected to one input (A) of the full-adder FA-1, so the input (A) receives the value of $\mathrm{A}_{0}$. Similarly, the full-adder FA-2, FA-3, and FA-4 receive the values of $A_{1}, A_{2}$, and $A_{3}$ as one input (A), respectively. Now in FA-1, the carry in $\left(\mathrm{C}_{\mathrm{in}}\right)$ is 1 (as the mode $\left.(\mathrm{A} / \mathrm{S})=1\right)$, and the input $A$ receives the value of $0\left(\right.$ as $\left.A_{0}=0\right)$, and the input $B$ receives the value of 0 , which is the complement of $\mathrm{B}_{0}$ (as $\mathrm{B}_{0}=1$ ). According to the operational principle of full-adder, the output $S$ of FA- 1 is one $\left(\mathrm{D}_{0}=1\right)$ and the carry out is zero $\left(\mathrm{C}_{\text {out }}=0\right)$. Again in FA-2, $\mathrm{C}_{\mathrm{in}}=0$ (as $\mathrm{C}_{\text {out }}$ of the full-adder FA-1 is 0 ). The input A receives the value of $0\left(\right.$ as $\left.A_{1}=0\right)$ and the input $B$ receives the value of $1\left(\right.$ as $\left.B_{1}=0\right)$, so $D_{1}=1$ and $C_{\text {out }}=0$. Similarly in FA-3, $\mathrm{C}_{\mathrm{in}}=0$, and the input A receives the value of 1 (as $\mathrm{A}_{2}=1$ ), and the input B receives the value of 1 (as $\mathrm{B}_{2}=0$ ). Hence $\mathrm{D}_{2}=0$ and $\mathrm{C}_{\text {out }}=1$. Finally in FA-4, $\mathrm{C}_{\text {in }}=1$, the input A receives the value of $1\left(\right.$ as $\mathrm{A}_{3}=$ $1)$, and the input $B$ receives the value of $0\left(\right.$ as $\left.B_{3}=1\right)$, so $\mathrm{D}_{3}=0$ and $\mathrm{C}_{\text {out }}=1$, i.e., $\mathrm{D}_{4}=1$. So it generates the output $D$ as $10011\left(D_{4} D_{3} D_{2} D_{1} D_{0}\right)$. In this case the optical circuit uses 2's complement method of subtraction. As the final carry $\left(\mathrm{C}_{\text {out }}\right)$ from FA-4 is one $\left(\mathrm{D}_{4}=\right.$ 1), that means the result will be positive and hence the final carry $\left(\mathrm{D}_{4}\right)$ is to be discarded. Here, the final result is positive and its value is $0011\left(D_{3} D_{2} D_{1} D_{0}\right)$, which verifies subtraction operation. Now if we consider $\mathrm{A}=$


Fig. 6. Simulated wave form of 4-bit A/S.
$1001\left(\mathrm{~A}_{3} \mathrm{~A}_{2} \mathrm{~A}_{1} \mathrm{~A}_{0}\right)$ and $\mathrm{B}=1100\left(\mathrm{~B}_{3} \mathrm{~B}_{2} \mathrm{~B}_{1} \mathrm{~B}_{0}\right)$, the optical circuit generates the output D as $01101\left(\mathrm{D}_{4} \mathrm{D}_{3} \mathrm{D}_{2} \mathrm{D}_{1} \mathrm{D}_{0}\right)$. As the final carry is zero $\left(D_{4}=0\right)$, that means the result will be negative and hence the final carry $\left(\mathrm{D}_{4}\right)$ is to be discarded. So the final result is negative and its value is 0011 (2's complement of 1101). The simulated wave form is given in Fig. 6.
In conclusion, the significant advantage in this proposed scheme is that the proposed A/S unit can perform two different operations (addition and subtraction) which are all-optical in nature. The same architecture can be used for different purposes. This scheme can be easily and successfully extended and implemented for any higher number of input digits by proper incorporation of TOAD based XOR and full-adder. Arithmetic operations can be conducted here between any two large shaped data. Computer simulation results confirming described methods are given in this letter. It is important to note that the above discussions are based on a simple model. To experimentally achieve the result from the proposed scheme, some design issues have to be considered. For example, walk-of problem due to dispersion, polarization properties of fiber, predetermined values of the intensities/wavelength of the laser light for the control and incoming signals, introduction of filter, intensity losses due to fiber couplers, etc. Because of the small size of TOAD, the walk-off between the control and incoming signal may not be a great problem. Lasers of wavelength at 1557 and 1549 nm can be used as the incoming and control signal, respectively. Here,
"PLS" can be a mode-locked $\mathrm{Er}^{3+}$-doped fiber pulsed laser (EDFL) source (unpolarized/partially polarized) of $1557-\mathrm{nm}$ wavelength. The control signal is also a 1549nm EDFL. Optical circulator can be used to isolate the reflected pulse. Band pass filter (BPF) passes the signal of $1557-\mathrm{nm}$ wavelength and blocks the signal of $1549-\mathrm{nm}$ wavelength. Here the TOAD loop length is less than 0.5 m , SOA is InGaAsP traveling wave semiconductor optical amplifier of $500-\mu \mathrm{m}$ length with low polarizing sensitive (BT\&D SOA 3200). Intensity losses due to couplers in interconnecting stage may not create much trouble in producing the desired optical bits at the output as the whole system is digital one and the output depends only on the presence or absence of the light.

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