

Technology challenges for monolithically integrated waveguide demultiplexers

Invited Paper

Lech Wosinski^{1*}, Liu Liu², Ning Zhu¹, and Lars Thylen¹

¹Department of Microelectronics and Applied Physics, Royal Institute of Technology (KTH), Electrum 229, SE-164 40, Kista, Sweden, Joint Research Center of Photonics of the Royal Institute of Technology and Zhejiang University

²INTEC Department, Photonics Research Group, Ghent University-IMEC, St-Pietersnieuwstraat 41, 9000 Ghent, Belgium

*E-mail: lech@kth.se

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A short overview of integrated waveguide demultiplexers for different applications in future highly integrated optical communication systems is presented. Some fabricated devices based on amorphous silicon nanowire technology are described.

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Optical multiplexers and demultiplexers nowadays find many applications having different functions in wavelength division multiplexing (WDM) networks. Depending on the channel spacing, they have been classified as: wide wavelength division multi/demultiplexer (WWDM) with ≥ 50 nm channel spacing, coarse wavelength division multi/demultiplexer (CWDM) with < 50 nm channel spacing, and dense wavelength division multi/demultiplexer (DWDM) with ≤ 8 nm channel spacing. WWDMs are commonly used as triplexers for example in passive optical networks for FTTx (fiber-to-the-home, etc.) applications. In this case, they are designed to combine or separate three channels at wavelengths of 1310, 1490, and 1550 nm carrying data, video, and voice signals onto one single optical fiber. CWDMs combine usually up to 16 wavelengths onto a single fiber. It is a cheap solution due to the fact that the large channel separation eliminates expensive stabilized narrow-band lasers. CWDM technology uses an International Telecommunication Union (ITU) standard 20-nm spacing between the wavelength from 1310 to 1610 nm. DWDMs combine up to 64 wavelengths or more onto a single fiber. DWDM technology uses an ITU standard 100 GHz (0.8-nm channel spacing between the wavelengths) or less, arranged in several bands in the optical communication window of 1500–1600 nm. This is the most expensive solution, but gives the highest network capacity, suitable for applications where there are many users sharing the costs. DWDMs are mainly used for long haul metro area networks (MANs) and wide area networks (WANs).

There are many techniques available today for the realization of these components including thin film filters, Bragg gratings, arrayed waveguide gratings (AWGs), and echelle gratings (also called etched diffraction gratings, EDG). The last two solutions appear to be most suitable for wafer scale mass production. Both of them have been fabricated using different material platforms, including silica-on-silicon, III-V materials, as well as silicon-based technology. The Royal Institute of Technology (KTH) in Sweden has a long tradition in this work. Figure 1 shows

a series of 32-channel AWGs with 0.8-nm channel spacing, realized in SiO₂/Si material structure, fabricated at KTH^[1]. In Fig. 2, two of the components of the optical code-division multiple-access (OCDMA) structure are AWGs, realized in cooperation with another KTH group in InP technology^[2].

An AWG^[3] is composed of input and output waveguides coupled to an array of waveguides (regularly arranged with increasing lengths) through two focusing slab waveguides, free propagation regions (FPRs), where light is not confined laterally and therefore diverges or converges in the lateral direction. An optical beam entering

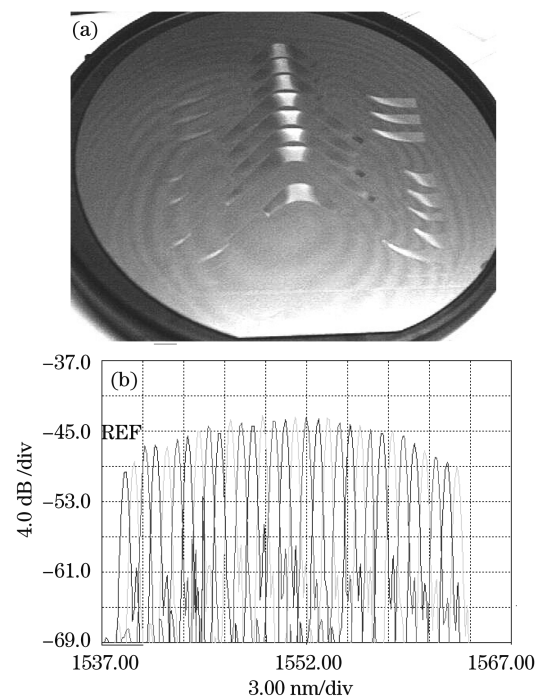


Fig. 1. 32×32 AWG in SiO₂/Si technology. (a) Fabricated devices, (b) AWG transmission spectrum.

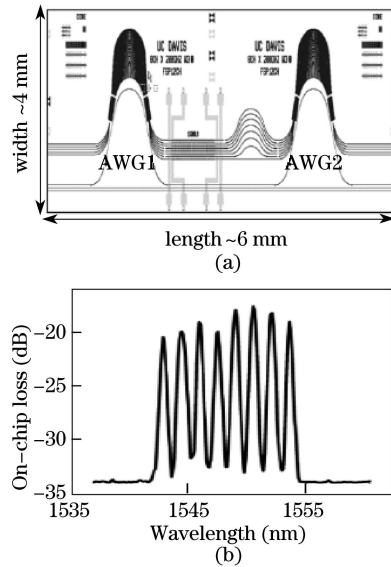


Fig. 2. InP-based OCDMA encoder. (a) Chip layout, (b) encoder transmission spectrum^[2].

the 1st FPR (input FPR), through the input waveguide, spreads by diffraction and continues through the array of waveguides. Due to the constant path length difference between adjacent waveguides, after passing through the array, the different wavelength signals that reach the output slab waveguide interfere in different directions in the output FPR towards output waveguides. In an EDG device^[4], the incident light from an input waveguide is diffracted by the grating and then reflected towards several output waveguides corresponding to different wavelengths. In both AWG and EDG, the focusing of diffracted wavelengths into different output waveguides is based on Rowland geometry^[5,6].

Silica-on-silicon technology has shown the ability to keep high performance even for devices with high levels of integration. Nevertheless, a common drawback of this technology is the overall size of the components, mostly limited by the large bend radius. This limitation dictated by a low refractive index difference between the core and the cladding of the device and so, low light confinement, causes that a single multichannel AWG has a size of several square centimeters and the integration of more complex structures is often difficult on a single wafer. To increase the integration density for future WDM systems, a considerable size reduction is necessary.

Technology based on III-V semiconductors has gained a lot of attention as it is possible to realize almost all important building blocks for optical communication in this material: passive waveguides and wavelength selective devices, light sources, switches, modulators, and detectors. However, for very small structures, high index contrast to the air or dielectric overcladding is not sufficient as light leaks out of the bends to the buffer or substrate because of the low index contrast between substrate and epitaxial grown materials. III-V semiconductor-based structures suffer also for higher losses and higher material cost. Moreover, their material technology is more complex in comparison with other technologies based on silicon wafer.

Silicon is an inexpensive and the most widely used

semiconductor material in current electronic devices. For photonic applications, it is important that silicon is transparent for the optical communication window and has a high refractive index of 3.5 in comparison with silica ($n=1.5$), which can be used as surrounding media.

To use silicon as a light guiding material for passive devices, the main constraints until recently were relatively high propagation losses and high fiber-to-waveguide in-coupling losses. The general trend towards high integration together with progress in fabrication techniques resulted in the development of silicon photonic wire waveguides, formed as silicon strips on a silica layer. The strips have a cross section of only 250×500 (nm). This technology allows for fabrication of the next generation photonic devices. Although the losses of the silicon material have not been greatly reduced, being still about one order of magnitude higher than those of silica based channel waveguides, the enormous component size shrinkage due to a very high refractive index contrast in all directions obtained using silicon results in a considerable decrease of losses per component. Simultaneously the problem of fiber-to-waveguide in-coupling losses has been solved using advanced tapers and mode converters. The possibility to merge both electronics and photonics in the same chip and the presence of a large silicon industry that can take over the mass production became very attractive issues.

Most of the fabricated passive nanophotonic devices are formed using silicon-on-insulator (SOI) technology, where commercially available SOI wafers are normally used. In this letter, all the presented devices have been fabricated based on amorphous silicon (a-Si) platform, which is a technique developed at KTH^[7]. This technique, where all the layers are plasma enhanced chemical vapor deposition (PECVD) deposited, allows for much more flexibility and variations in the design of Si-based optical components in comparison with standard SOI structures.

In this technology, after the deposition of SiO_2 buffer layer and a-Si core layer, the devices are patterned by e-beam lithography and subsequently etched with inductively coupled plasma reactive ion etching.

In these sub-micron size structures, the fabrication accuracy has a very critical influence on the performance of the devices. High contrast makes that waveguide losses are very sensitive to the scattering due to the roughness on the core-cladding interface. Especially, the sidewall surfaces after etching the waveguide profile are crucial for the final quality of the device. Both lithography and etching can have influence on the sidewall roughness and so both these steps should be optimized. The sidewall roughness can be also improved after etching by slight thermal oxidation of the etched silicon profiles.

As an example for DWDM, a 5×5 compact AWG with 1.6-nm channel spacing was fabricated^[7]. The device and its transmission spectrum are shown in Fig. 3 and its detailed structural parameters are presented in Table 1 (for AWG1.6).

As an example for CWDM, a 4×4 AWG with an ultra-small size of $40 \times 50 \mu\text{m}^2$ and channel spacing of 11 nm has been fabricated^[8]. The device and its transmission spectrum are shown in Fig. 4 and its detailed structural parameters are presented also in Table 1 (for AWG11).

For the realization of a WWDM, we chose a triplexer with an EDG solution. As the spectral range here is very wide stretching from 1310 to 1550 nm, it is convenient and desirable, taking into consideration the channel uniformity, to not put all 3 channels into one free spectral range (FSR). Here we used a cross-order solution^[9], which utilizes different diffraction orders for different wavelengths. We chose a diffraction order 5 for channel 1 (1550 nm) and channel 2 (1490 nm), while a diffraction order 6 for channel 3 (1310 nm). The thickness of the Si layer is 250 nm and the footprint of the device (not

including output waveguides) is only 150×120 (μm). Figure 5 shows the fabricated device and the spectral results of the triplexer and its detailed structural parameters are presented in Table 1. This kind of component has been for the first time realized as a nanowire device based on α -Si platform^[10].

Usually SOI-based optical components are polarization sensitive as it is in the case of the silicon-based demultiplexers presented here. If necessary, polarization diversity scheme can be applied, which can double the size of the component, although it still remains very compact.

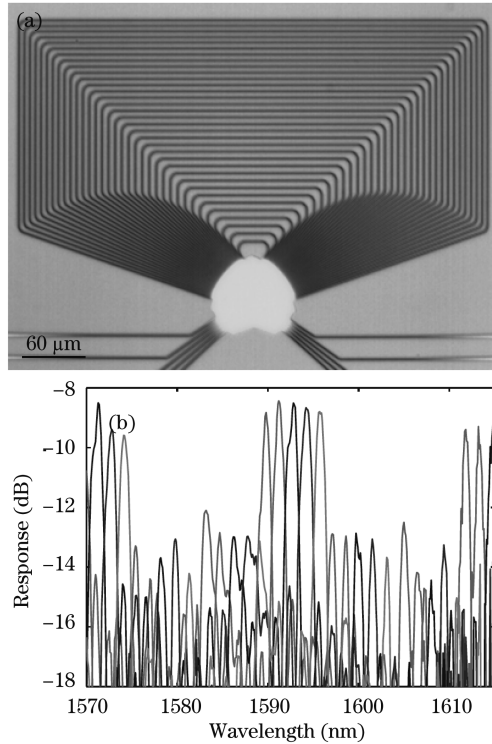


Fig. 3. DWDM based on 5×5 AWG in α -Si technology. (a) Fabricated device, (b) transmission spectrum.

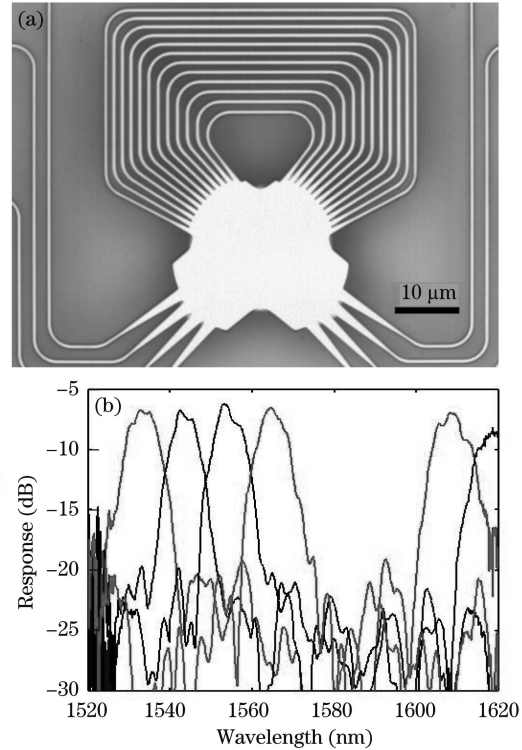


Fig. 4. CWDM based on 4×4 AWG in α -Si technology. (a) Fabricated device, (b) transmission spectrum.

Table 1. Designed Structural Parameters and Measured Spectral Characteristics for TE Polarization

Parameter	AWG1.6	AWG11	EDG
Waveguide Dimension (nm^2)	500×250	500×250	500×250
Number of Arrayed Waveguides	34	12	—
Number of Channels	5×5	4×4	1×3
Constant Length Difference ΔL (μm)	24.9	7.2	—
Diffraction Order	42	12	5 and 6
FPR (Focal) Length (μm)	50	20	—
Output Waveguide Width at FPR (μm)	1.5	1.5	—
Output Waveguide Spacing at FPR (nm)	350	500	—
Arrayed Waveguide Width at FPR (nm)	950	750	—
Arrayed Waveguide Spacing at FPR (nm)	50	50	—
Total Size (μm^2)	320×270	40×50	150×130
Channel Spacing (nm)	1.5	10.7	180, 60
FSR (nm)	21.7	75	172
Insertion Loss (dB)	~ -8.5	~ -6	~ -10
Crosstalk (dB)	~ -7	~ -14	~ -15

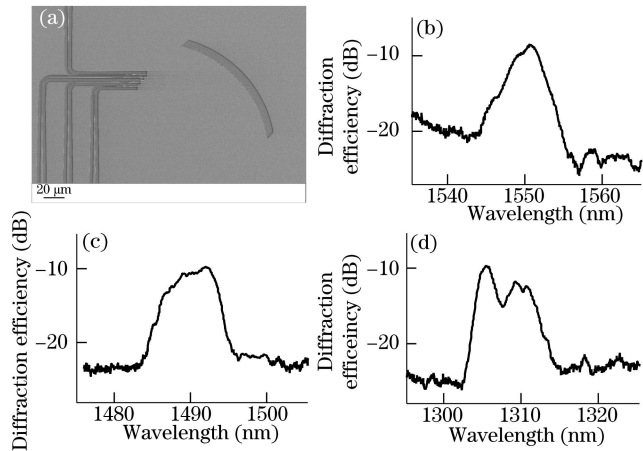


Fig. 5. WWDWM based on EDG in α -Si technology. (a) Fabricated device; (b)-(d) transmission spectra: (b) channel 1 for order 5, (c) channel 2 for order 5, and (d) channel 3 for order 6.

In conclusion, we have presented a number of solutions for the realization of integrated waveguide demultiplexers in different material structures. Silicon nanowire-based technology is an attractive way towards highly integrated systems with the capacity for wafer scale mass production compatible with microelectronics. The parameters of the fabricated devices are in many cases not sufficient for practical applications, but the technological improve-

ments are still possible that should allow to match the market demands.

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