Reverse current reduction of Ge photodiodes on Si without post-growth annealing

Invited Paper

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A new approach to reduce the reverse current of Ge pin photodiodes on Si is presented, in which an i-Si layer is inserted between Ge and top Si layers to reduce the electric field in the Ge layer. Without post-growth annealing, the reverse current density is reduced to ∼10 mA/cm^2 at −1 V, i.e., over one order of magnitude lower than that of the reference photodiode without i-Si layer. However, the responsivity of the photodiodes is not severely compromised. This lowered-reverse-current is explained by band-pinning at the i-Si/i-Ge interface. Barrier lowering mechanism induced by E-field is also discussed. The presented "non-thermal" approach to reduce reverse current should accelerate electronics-photonics convergence by using Ge on the Si complementary metal oxide semiconductor (CMOS) platform.

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Ge photodetectors (PDs) on Si are promising for high-performance and yet, cost-effective communication and computation on the Si complementary metal oxide semiconductor (CMOS) platform[1]. Despite 4.2% of lattice mismatch between Si and Ge, both materials belong to group IV and thus, there is no concern about inter-contamination. In other words, Ge PDs on Si have good material compatibility. Furthermore, at near infrared (NIR, 1300−1550 nm in wavelength) range, Si is completely transparent, while Ge has large absorption coefficient (∼10^3 cm^{-1}). Therefore, this material system has gained technological importance in photonics-electronics (P-E) convergence. One of the practical applications is optical clocking[2], where the high-frequency clock signal is distributed through Si waveguides and the optical signal is converted to an electric one at Ge PD. In this application, the arriving light intensity at the PD is extremely small. Therefore, high sensitivity is required. In order to enhance sensitivity which can be represented as signal-to-noise ratio (SNR), reverse leakage current should be sufficiently low. The key component in optical clocking is waveguide-integrated PDs, which have been demonstrated by many groups[3,4]. Their results of leakage current density at the reverse bias of 1 V are 130 and 1.43 A/cm^2[3,4]. These values are considerably large for operation with high SNR.

Giovane *et al*. have investigated about the leakage generation, associating it with threading dislocation (TD) density[5]. The photodiode had a pin structure with $Si_{0.5}Ge_{0.5}$ epi-layer on Si, which contained plenty of TDs. They found that there was a linear correlation between reverse leakage current and TD density. From this relation, it is predicted that the reverse leakage current can be reduced by decreasing TD density through thermal annealing. In fact, some have reported Ge PDs with nearly ideal responsivity spectrum with a relatively low reverse current by annealing their Ge at ∼900 °C[6,7]. This post-growth annealing has reduced TD density from ∼10^9 to ∼10^7 cm^{-2}. However, such high-temperature annealing impedes the integration of Ge photodiodes to Si electronics because it limits the process of Ge introduction only to the front-end step of the standard CMOS process-flow. In fact, there are non-thermal ways to achieve Ge epi-layers with low TD density such as by using lateral overgrowth[8]. However, there is a difficulty to use such a Ge layer in the PD fabrication process because of the highly defective Si/Ge interface. Therefore, it is advantageous to reduce leakage current in spite of the presence of large TD density, i.e., by using as-grown Ge epi-layer on Si.

TDs in Ge act as a generation center, whose energy-level is located at the mid-bandgap of Ge[9]. Such generation can be enhanced as E-field strength (F) increases. Therefore, it is possible to reduce leakage current by lowering F at a defective Ge layer. There are several models to explain this mechanism such as the Poole-Frenkel (P-F) effect[10], Schottky barrier lowering (SBL)[11], or band-to-band tunneling (BBT)[12]. For the deep-level defects such as TDs, SBL cannot be an appropriate model. Furthermore, BBT cannot explain the mechanism for Ge PD either, because this is dominant at room temperature (RT) only when F is greater than 700 kV/cm[11]. This F value exceeds the breakdown voltage for Ge. Therefore, the leakage generation in Ge PD must be strongly associated with F according to the P-F model.

In this letter, we propose a non-thermal approach to reduce the reverse leakage current by controlling the E-field inside the Ge layer. The new approach has successfully reduced the reverse current, whereas the spectral responsivity is not severely compromised. In addition, we focus on explaining the mechanism of lowered leakage current, based on the P-F effect.

The reverse current density J_r (A/cm^2) can be expressed as

$$J_r = \frac{q\, n_i\, d}{\tau_{SRH}}\Gamma, \tag{1}$$

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where q denotes the elemental charge, $n_{\rm i}$ is the intrinsic carrier density, d is the depletion layer width, Γ is the field enhancement factor, and $\tau_{\rm SRH}$ is the lifetime in terms of the Shockley-Read-Hall (SRH) theory expressed by

$$\tau_{\rm SRH} = \frac{1}{\sigma\, v_{\rm th}\, N_{\rm TD}\, N_D}. \quad (2)$$

σ denotes the capture cross section, $v_{\rm th}$ is the thermal velocity of carriers, $N_{\rm TD}$ is the areal-density ($\rm cm^{-2}$) of TDs, and N_D represents the line-density ($\rm cm^{-1}$) of the generation centers along TDs. Here, we assume that TDs serve as a dominant generation center. When there is no enhancement for reverse leakage current by electric field strength, the Γ value in Eq. (1) is 1. However, Γ is larger than 1 when the electric field promotes the leakage-current generation. The Γ dependency on the E-field strength F can be associated with several mechanisms such as P-F effect or defect assisted tunneling (DAT), etc.[13]

Figure 1 shows $J_{\rm r}$ as a function of TD density $N_{\rm TD}$ at -1 V with reported results found in literatures as well as our data[5,7,14,15]. Note that the reported PDs have similar structure to ours, i.e., vertical pin photodiode and depletion region exist inside a defective Ge layer. Additionally, $J_{\rm r}$ has to be normalized by thickness of the Ge layer (i.e., depletion width) as shown in Eq. (1). In typical current-voltage (I-V) curves of Ge PDs without post-growth annealing, the reserve leakage current drastically increases as the reverse bias increases[15]. This trend strongly suggests that the generation of leakage current due to presence of TDs is enhanced by F. Suppose that depletion region exists only inside defective Ge. Γ is a constant value larger than 1, which is determined by F. Here, F is merely a function of reverse bias and Ge thickness. In that case, $J_{\rm r}$ is linearly proportional to $N_{\rm TD}$, as shown by the dotted line in Fig. 1. However, we observed significant reduction of reverse leakage current by introducing intrinsic (i-) Si layer. We believe that this is due to the low effective F in Ge. In this letter, we primarily focus on the mechanism of low F in Ge by i-Si insertion and dependence of reverse leakage current on F.

To lower F in Ge, we have designed the cross-sectional structure of the photodiodes with a thin i-Si layer inserted between the i-Ge layer and the n-Si layer, as shown in Fig. 2(a). The reference photodiode without the i-Si layer as shown in Fig. 2(b) was also fabricated for comparison. Considering the Fermi level pinning due to the presence of negatively charged defects at i-Si/i-Ge interface (acceptor-like interface)[16], the band structure of the photodiodes with and without the i-Si layer can be simulated (We used one-dimensional device simulator *PC1D* for the band structures and the responsivity spectra). The calculated band structures are shown in Figs. 2(c) and (d). Here, the charge density of acceptor-like $\rm i-Si/i-Ge$ interface is assumed to be 3×10^{11} $\rm cm^{-2}$. We will discuss on how this value is determined later. Compared with the reference Ge photodiode, F of the Ge layer with i-Si layer is reduced and almost flattened at 0 V. Therefore, it is suggestive from the simulation that F can be lowered by making i-Si/i-Ge interface remain undoped, which makes it possible to lower F even smaller than the built-in F of the reference photodiode.

Epitaxial growth was done in an ultrahigh vacuum chemical vapor deposition (UHV-CVD) reactor with a base pressure of 5×10^{-7} Pa. Four-inch boron-doped p-Si(100) wafer with resistivity of 0.01−0.02 Ω·cm were used as a starting substrate. GeH_4 and Si_2H_6 were used as precursors. A ∼30-nm-thick Ge buffer layer was grown on the substrate at 370 °C, followed by the growth of a 600-nm-thick Ge layer at 600 °C. Without any

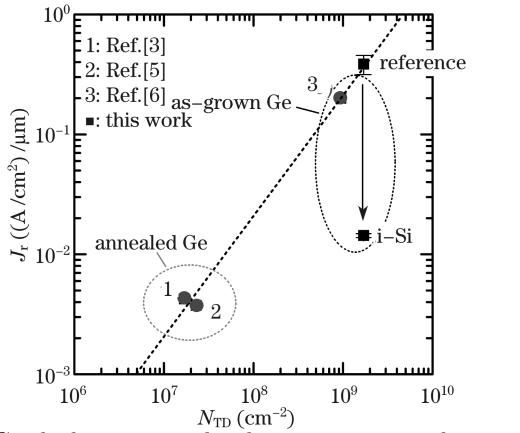

Fig. 1. Ge-thickness-normalized reverse current density ($J_{\rm r}$) at reverse bias of -1 V as a function of TD density ($N_{\rm TD}$).

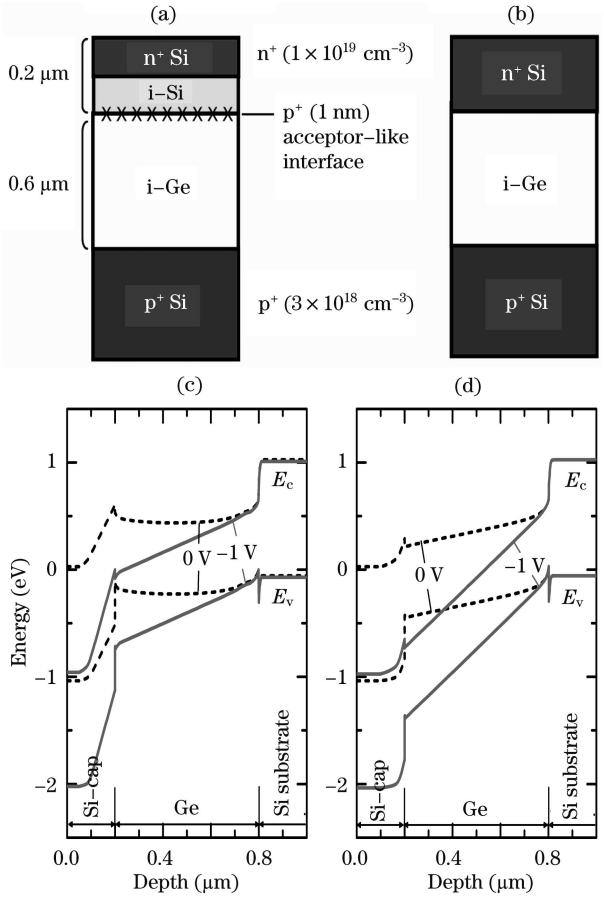

Fig. 2. Schematic illustration of fabricated Ge photodiodes of (a) "i-Si" and (b) "reference" photodiodes and calculated band structures for (c) "i-Si" and (d) "reference" photodiodes. Here, we assume 3×10^{11} $\rm cm^{-2}$ as the surface density of negatively charged defects between i-Si and i-Ge. $E_{\rm c}$ and $E_{\rm v}$ stand for conduction and valence bands, respectively.

interruption, a 200-nm-thick Si-cap was grown on the as-grown Ge surface at 600 °C. A 300-nm-thick SiO_2 layer was deposited on the as-grown epi-films by sputtering and then patterned by photolithography to partly remove SiO_2. The square-shaped window defines the photodiode size and it ranges from 20×20 to 500×500 (μm^2) in area. Phosphorous (P) was implanted at the peak concentration of 10^{19} cm^{-3} into the exposed Si patterns to form n-Si layer of the photodiode. Two acceleration voltages for the P implantation were chosen as 20 and 70 keV, corresponding to the peak depths of 20 and 100 nm from the Si-cap surface, respectively. As a result, P ion-profile was varied to fabricate two types of photodiodes: one was an n-region only near the Si-cap surface and the rest of Si-cap layer remained undoped, referred to as "i-Si" photodiode; the other has no i-Si layer remaining at the Si-cap layer, referred to as "reference" photodiode. The cross-sections of the photodiodes are illustrated in Figs. 2(a) and (b). No post-growth annealing was employed except for the recrystallization annealing after P implantation at 650 °C for 30 min in order not to affect N_{TD}. After the recrystallization annealing, Al was deposited and patterned to define electrodes for the probe measurement. As-fabricated photodiodes were characterized by I-V and spectral responsivity ($R(\lambda)$). A direct current (DC) source monitor (Agilent 4156C) was used for the I-V measurement. For the $R(\lambda)$ measurement, monochromatic light from tungsten-halogen lamp was directed at normal incidence to the aperture of photodiodes of 500×500 μm^2 in area. In order to estimate N_{TD} in the Ge layer by wet chemical etching, another Ge epi-film was deposited on Si substrate without the top Si-cap. Etchpit density (EPD) was counted on the scanned images by atomic force microscopy (AFM). The average EPD was 1.7×10^9 cm^{-2}, which we refer to as N_{TD} in the Ge layer of the both "i-Si" and "reference" photodiodes.

Figure 3 shows typical I-V curves of "i-Si" and "reference" photodiodes. The reverse current of both photodiodes is dependent on quality of the Si and Ge epi-layers based on the fact that the reverse current is proportional to the area of the photodiodes, rather than to the perimeter. The reverse current of the "i-Si" photodiode is clearly lower than that of the "reference" photodiode. The average reverse current density was measured to be 8.58 mA/cm^2 (i.e., 14.3 (mA/cm^2)/μm) for the "i-Si" photodiodes at −1 V, whereas it was 230 mA/cm^2 (i.e., 384 (mA/cm^2)/μm) for the "reference" one. It becomes evident from Fig. 1 that there is linear correlation between J_r and N_{TD} when depletion region exists in a defective Ge layer. J_r of the "i-Si" photodiodes in spite of N_{TD} of $\sim10^9$ cm^{-2} is comparable to that of the annealed photodiode with N_{TD} of $\sim10^8$ cm^{-2}. This result indicates that inserting i-Si layer at the interface with i-Ge is effective to reduce the reverse current. We believe that this result is attributed to low F in Ge of the "i-Si" photodiodes due to band-flattening, which significantly deactivates TDs as a source of leakage current.

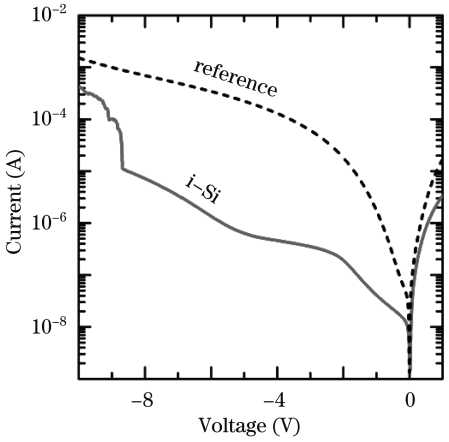

Fig. 3. $I-V$ curves of the "i-Si" photodiode and the "reference" one. The device size is 20×20 μm^2.

Figure 4(a) shows the responsivity-spectra ($R(\lambda)$) of the "i-Si" photodiode. Although the responsivity is quite low at 0 V, it increases as reverse bias increases and begins to saturate even at a low reverse bias of 0.5 V. The responsivity of the "i-Si" photodiode at −1 V is 70 mA/W at 1550 nm. That corresponds to ∼93% external quantum efficiency, which is comparable to the "reference" photodiodes. We believe that low responsivity at 0 V is attributed to low F, which hinders the photogenerated carriers to be collected.

Now, we discuss the effect of the band-flattening of "i-Si" photodiodes on responsivity so that we can theoretically determine F at both i-Ge and i-Si layers. It is difficult to measure F in each layer experimentally. Therefore, we used $PC1D$ simulator. By calculating responsivity at normal incidence of light when varying both reverse bias and charge density at i-Si/i-Ge interface for the "i-Si" photodiode, we could determine the charge density and eventually, could calculate the band-structure for each device, as in Fig. 2. As shown in Fig. 4(b), the measured responsivity spectra are best reproduced when the negative charge density at i-Si/i-Ge interface is 3×10^{11} cm^{-2}, which has been used for calculation of band structures in Figs. 2(c) and (d). According to the report by Masini *et al.*, the charge density of 5×10^{13} cm^{-2} should be assumed for Ge/Si(100) hetero-interface, based on 4.2% lattice-mismatch[17]. However, our estimation for the charge density at i-Si/i-Ge interface is much smaller than their estimation. In fact, Masini *et al.* investigated the interface between a Ge buffer layer grown at low temperature (∼350 °C) and a Si substrate. Consequently, the buffer layer must contain a large

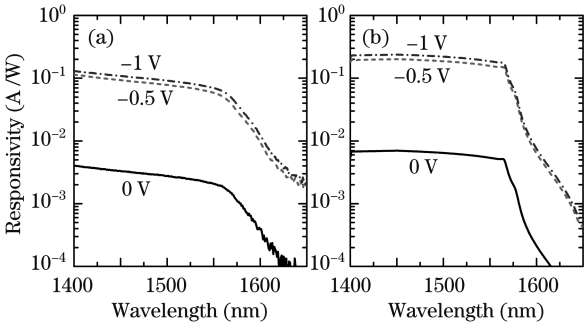

Fig. 4. (a) Measured responsivity spectra of the "i-Si" photodiode and (b) calculated one with 3×10^{11} cm^{-2} of negative charge density at i-Si/i-Ge interface.

number of defects. Compared with their low-temperature buffer, our Si-cap/Ge interface grown at 600 °C is less defective. In fact, this claim could be confirmed by cross-sectional transmission electron microscopy (TEM). We believe that our estimation for charge density at i-Si/i-Ge interface has played a crucial role in determining the band-structures of our photodiodes. Note that the F values used in this letter were estimated from the calculated band-diagrams, as shown in Figs. 2(c) and (d).

In order to investigate the mechanism for the lowered reverse leakage current, we have studied correlation between reverse current $I_{\rm r}$ and E-field strength F. Based on the P-F effect, the relation between them is given as

$$I_{\rm r} \propto F \exp\left(\frac{q}{kT}\sqrt{\frac{qF}{\pi\varepsilon}}\right), \tag{3}$$

where q denotes the elemental charge, k is BoltZmann's constant, T is absolute temperature, and ε is the permittivity of the material under E-field.

Figure 5 shows the semi − log plot for $I_{\rm r}/F$ and $F^{1/2}$ of both the "i-Si" and the "reference" photodiodes. For the "reference" photodiode, the linear-fitting slope (0.270) of $I_{\rm r}/F$ and $F^{1/2}$ shows a good agreement with the theoretical value (0.281) of P-F effect. Therefore, it appears that the reverse current due to TDs in Ge is affected by F according to P-F barrier lowering. In contrast, for the "i-Si" photodiode, there are two regimes. One has a smaller slope at smaller F, the other has a larger slope and ultimately reaches the $I_{\rm r}$ of the "reference" photodiode at larger F. In fact, the I-V curve of the "i-Si" photodiode in Fig. 3 shows a sudden rise around −9 V, which appears to be a breakdown behavior. This reverse bias (−9 V) corresponds to the F value of ∼100 kV/cm for the "i-Si" photodiode in Fig. 5, which is known as a breakdown voltage of Ge. This result strongly suggests that our estimation of F in Ge from the $PC1D$ simulation is reliable. In addition to the "i-Si" photodiode with F of i-Ge in Fig. 5, we normalized the plot by substituting to F in the i-Si layer. The slope at the low F regime is well fit to P-F analysis. This suggests that at low F regime, the reverse leakage current is mainly contributed by generation from i-Si layer under strong F in accordance with P-F effect. In fact, the overlying Si-cap appears extremely defective from the TEM observation. Consequently, these defects are activated as a generation source when F increases. Therefore, it would be the key to further reduction of $I_{\rm r}$ to achieve the epi-growth of high-quality Si-cap on Ge. However, such reduction of $I_{\rm r}$ by generation from i-Si is possible only when the band-pinning takes place at the i-Si/i-Ge interface. Here, we believe that the negatively-charged interface with 3×10^{11} cm^{-2} as estimated from Fig. 4 is deactivated under strong F. As a result, F starts to exert in the i-Ge layer and thus, causes a breakdown. We need to clarify the mechanism for this. Other remaining tasks are to precisely measure the F, e.g., by electroreflectance (ER) or photoreflectance (PR) and to perform I-V measurement with varying temperature in order to determine the activation energy of leakage generation. We will report more detailed analysis elsewhere.

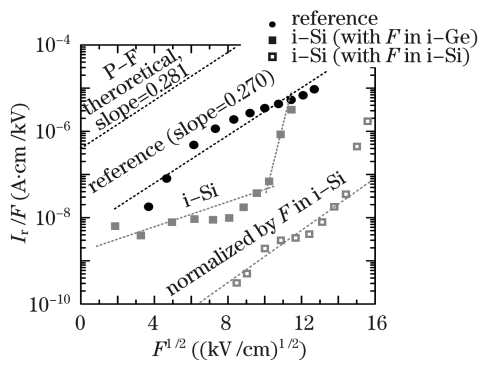

Fig. 5. Electric field strength F dependence of the reverse current $I_{\rm r}$, i.e., semi-logplot of $I_{\rm r}/F$ versus $F^{1/2}$.

The new approach presented in this paper should be an enabler to lower the process temperature for low-leakage Ge photodiode integrated on the Si CMOS platform. If Ge could be grown under 450 °C with $in-situ$ doping, the Ge photodiodes can be readily integrated with electronics at the "back-end" process.

In conclusion,we have proposed a new approach of Ge photodiodes on Si to reduce the reverse current without a high temperature post-growth annealing. We have demonstrated the photodiodes on Si consisting of Ge and over-lying i-Si layer. In spite of the high $N_{\rm TD}$ (∼ 10^9 cm^{-2}) in Ge, we have obtained reverse current density as low as ∼10 mA/cm^2 with comparable responsivity. We have interpreted these results in terms of Fermi level pinning due to negatively charged i-Si/i-Ge interface. The presented approach along with low reverse current should accelerate the integration of Ge photodiodes on Si without a high-temperature annealing.

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