

Vertical cavity surface emitting lasers fabricated with pulsed anodic oxidation

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The technique of pulsed anodic oxidation is adopted in the fabrication of 980-nm bottom-emitting vertical-cavity surface-emitting lasers. A high-quality native oxide current blocking layer is formed with this method. A significant reduction of threshold current and a distinguished device performance are achieved. The threshold current of large aperture devices with active diameter up to 400 μm is as low as 0.45 A at room temperature, which is substantially lower than the lasers fabricated by SiO_2 sputtering. The maximum continuous-wave output power is 0.83 W. The lasing peak wavelength is 990.2 nm, and the full width at half-maximum is 0.9 nm. Low lateral divergence angle of 15.3° and vertical divergence angle of 13.8° are obtained.

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Since vertical-cavity surface-emitting laser (VCSEL) was firstly proposed in 1977, great progresses have been made on it. VCSEL devices of different characteristics have appeared, for example, devices of low threshold^[1], room temperature continuous-wave operation and wavelength from visible to infrared, etc.^[2-4]. Also, owing to its merits such as low divergence angles compatible with optical fibers, on-wafer testing, inherent single longitudinal mode operation, and high-density two-dimensional (2D) arrays, VCSEL has emerged as the attractive light sources for optical interconnects^[5], data communications, optical storage, compact disc-read only memory, and digital video disc pickup head^[6], optical printing, and wavelength-division multiplexing.

The integration of optoelectronic devices based on planar configurations may only be realized if suitable methods are available to form insulating oxide layers of acceptable qualities on the surfaces of III-V semiconductors. This layer is conventionally formed by deposition of SiO_2 or Si_3N_4 with plasma enhanced chemical vapor deposition^[7]. However, the oxidation process is carried out at a typically high temperature from 400 to 650 $^\circ\text{C}$. Furthermore, SiO_2 reacts with Al when in direct contact with AlGaAs, and thus generates Si which behaves as an impurity source. Si_3N_4 , on the other hand, causes considerable strain^[8]. Alternatively, the pulsed anodization technique has recently attracted attention as a new way of forming current blocking layers for ridge-waveguide quantum well (QW) laser fabrication, since it has the advantages of low cost, high reliability, room temperature, self-aligned processing nature, and growth rate 10 times faster than anodization with constant voltage. The anodic oxide of GaAs has successfully been used to achieve impurity-free interdiffusion of GaAs/AlGaAs quantum wells^[9]. Moreover, the oxidation formed on $(\text{AlGa})_{0.5}\text{In}_{0.5}\text{P}$ has been shown to emit visible light during pulsed anodic oxidation (PAO)^[10]. AlGaAs diode lasers fabricated with pulsed anodic oxides had threshold current substantially lower than the lasers fabricated

with SiO_2 .

In this paper, we report the fabrication of 980-nm bottom-emitting VCSEL with high-quality native oxide current blocking layer formed by PAO. A significant reduction of threshold current density and a distinguished device performance are realized.

Figure 1 illustrates the configuration of the sample structure used in this work. The multi-layer wafer is grown by metal organic chemical vapor deposition on an n-GaAs substrate. The inner cavity consists of three 8-nm-thick $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ quantum wells embedded in 10-nm-thick GaAs barriers. Two $\text{Al}_x\text{Ga}_{1-x}\text{As}$ cladding layers are introduced on both sides of the active region to improve longitudinal carrier confinement and to make the cavity one wavelength large. The carbon-doped p-type distributed Bragg reflector consists of 30 pairs of $\text{Al}_{0.9}\text{Ga}_{0.1}\text{As}/\text{GaAs}$ with graded interface to reduce series resistance. The bottom Bragg reflector consists of 28 pairs silicon-doped $\text{Al}_{0.9}\text{Ga}_{0.1}\text{As}/\text{GaAs}$ quarter-wavelength layer pairs. There is a 30-nm-thick AlAs layer located between the active region and the top p-type mirror, which is to be oxidized and converted to Al_xO_y as the current confinement layer. The top 40-nm GaAs contact layer is doped to a concentration of $1 \times 10^9 \text{ cm}^{-2}$ to achieve a good ohmic contact.

Following the standard photolithography process the circular mesa with a depth down to the AlAs layer is

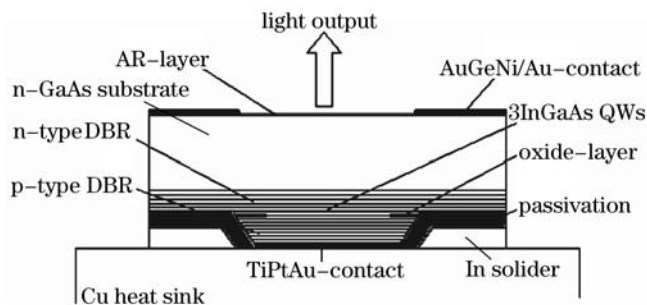


Fig. 1. Schematic diagram of the device structure.

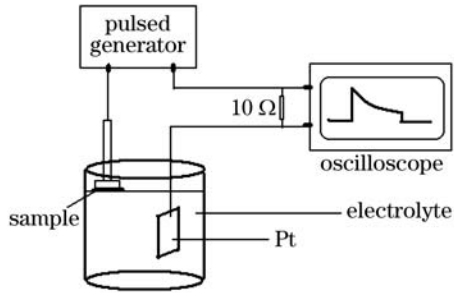


Fig. 2. Experimental setup for pulsed anodic oxidation.

formed by wet chemical etching. The exposed AlAs layer is laterally oxidized at an oxidation rate of $0.5 \mu\text{m}/\text{min}$ in the water vapor atmosphere. Nitrogen is used as the carrier gas at 420°C . With the photoresist on the top of the mesa, a native oxide layer is obtained by PAO method. Figure 2 schematically shows the anodization setup. The pulsed anodization is carried out at room temperature. The electrolyte is made of ethylene glycol, de-ionized water and phosphoric acid (40:20:1). A vacuum tube is used as the vacuum tweezer to conduct current and hold the sample with the surface dipped into the electrolyte. The solution, electrodes, and pulse generator are connected in series with small resistance (10Ω). The anodization is a reproducible oxidation-deoxidation process, so we use an oscilloscope to monitor the voltage variation to fix the terminal time of the anodization. The area uncovered by photoresist is anodized to form a native oxidation layer, with a pulse width of 1ms, a repetition of 100 Hz, and a pulse amplitude of 120 V. The anodization time is fixed at 2 min, at this time the trailing edge of the pulse no longer decreases. If staying in the electrolyte longer, the sample will be deoxidized. After rinsed by de-ionized water, the photoresist is removed by MF319 (a metal-ion-free photoresist developer), which can make the anodic oxides stable during the subsequent processing. Dried by N_2 , then Ti-Au-Pt-Au is evaporated as p-type contact to provide a homogeneous current distribution and serves as a metal pad for soldering. Before the deposition of an antireflection (AR) coating of HfO_2 film with quarter-wavelength thickness on the polished substrate, the GaAs substrate is thinned and chemically polished down to $180 \mu\text{m}$ in order to decrease the absorption losses. The n-type AuGeNi/Au substrate contact is evaporated surrounding the emission aperture formed by self-aligned lithography. After annealed at 420°C in nitrogen environment for 60 s, the whole chip is cleaved into single chips and soldered with p-side down with In-solder on metallized diamond heat sinks. Then the chip with diamond spreader is attached with indium paste on a copper submount.

To minimize the temperature difference between the copper submount and the active region, the devices are mounted on micro-channel cooler. Figure 3 shows the dependence of continuous wave (CW) light output and voltage on injection current for a $400\text{-}\mu\text{m}$ device fabricated by PAO. The maximum CW operation output power at room temperature is 0.83 W. The threshold current and threshold voltage are 0.45 A and 1.3 V. The differential resistance is 0.05Ω . The inset in Fig. 3 shows the

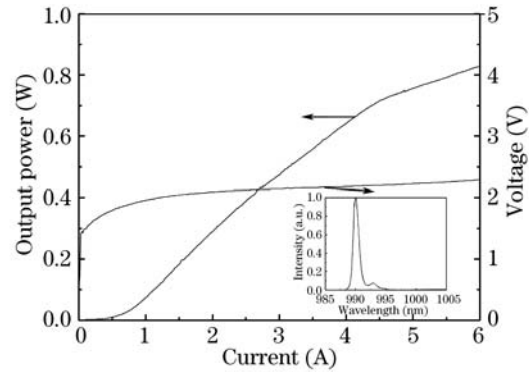


Fig. 3. Dependence of CW light output and voltage on injection current.

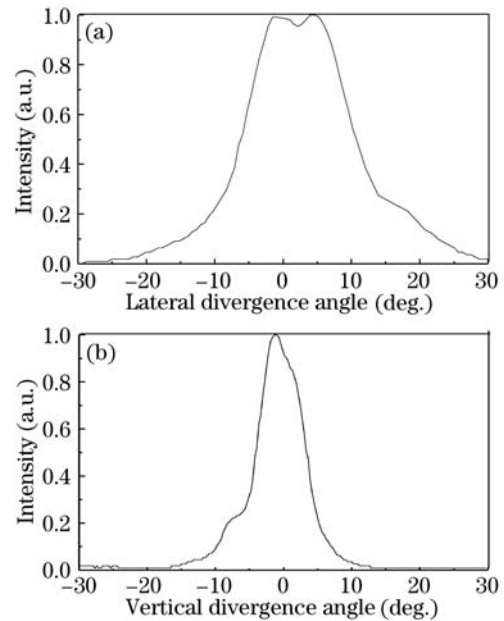


Fig. 4. Measured far-field patterns of bottom-emitting device.

lasing spectrum measured at an injected current of 6 A. The peak wavelength is 990.2 nm, and the full-width at half-maximum (FWHM) of the spectrum is 0.9 nm. The lateral divergence angle and vertical divergence angle are 15.3° and 13.8° without side-lobes at a current of 6 A as described in Fig. 4.

The device described above has high performance with low threshold current, low differential resistance and better far-field angle, which can be attributed to the isolation nature of PAO. Since the material is consumed in the anodic oxidation^[11], the hole cap is removed everywhere except under the mesa defined by photoresist. The consumption of the p^+ cap reduces lateral current spreading. So a better passivation of the side walls can be expected. Furthermore, the simple processing of PAO is also contributed to the better performance of the device by minimizing the possibility of process variations.

In conclusion, 980-nm bottom-emitting VCSEL is fabricated by PAO technique. A high-quality native oxide current blocking layer is formed and the threshold current has a significant reduction compared with the conventional VCSEL devices. The devices with the aperture size of $400 \mu\text{m}$ have the maximum CW output power of

0.83 W, the low threshold current of 0.45 A. The differential resistance is only 0.05Ω . At an injected current of 6 A, the peak wavelength is 990.2 nm, and the FWHM of the spectrum is 0.9 nm. Lateral divergence angle of 15.3° and vertical divergence angle of 13.8° without side-lobes are also obtained in the far-field distribution.

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References

1. D. L. Hiffaker, J. Shin, H. Deng, C. C. Lin, D. G. Deppe, and B. G. Streetman, *Appl. Phys. Lett.* **65**, 2642 (1994).
2. R. P. Schneider, Jr. and J. A. Lott, *Appl. Phys. Lett.* **63**, 917 (1993).
3. I. Burgaftman, J. R. Meyer, and L. R. Ram-Mohan, *IEEE J. Quantum Electron.* **34**, 147 (1998).
4. Koeth, R. Dietrich, and A. Forchel, *Appl. Phys. Lett.* **72**, 1638 (1998).
5. P. Schnitzer, M. Grabherr, R. Jager, F. Mederer, R. Michalzik, D. Wiedenmann, and K. J. Ebeling, *IEEE Photon. Technol. Lett.* **11**, 767 (1999).
6. H. K. Shin, I. Kim, E. J. Kim, J. H. Kim, E. K. Lee, M. K. Lee, J. K. Mum, C. S. Park, and Y. S. I, *Jpn. J. Appl. Phys.* **35**, 506 (1996).
7. J. C. Dymont, *Appl. Phys. Lett.* **10**, 84 (1967).
8. J. H. Marsh, *Semiconduct. Sci. Technol.* **8**, 1136 (1993).
9. S. Yuan, Y. Kim, C. Jagadish, P. T. Burke, M. Gal, J. Zou, D. Q. Cai, D. J. H. Cockayne, and R. M. Cohen, *Appl. Phys. Lett.* **70**, 1269 (1997).
10. C. C. Largent, M. J. Grove, D. A. Hudson, P. S. Zory, and D. P. Bour, *Solid-State Electron.* **38**, 1893 (1995).
11. H. Hasegawa and H. L. Hartnagel, *J. Electrochem. Soc.* **123**, 713 (1976).