Heteroepitaxial growth of InP/GaAs(100) by metalorganic chemical vapor deposition

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Using two-step method InP epilayers were grown on GaAs(100) substrates by low-pressure metalorganic chemical vapor deposition (LP-MOCVD). X-ray diffraction (XRD) and room-temperature (RT) photoluminescence (PL) were employed to characterize the quality of InP epilayer. The best scheme of growing InP/GaAs(100) heterostructures was obtained by optimizing the initial low-temperature (LT) InP growth conditions, investigating the effects of thermal cycle annealing (TCA) and strained layer superlattice (SLS) on InP epilayers. Compared with annealing, 10-periods $Ga_{0.1}In_{0.9}P$/InP SLS inserted into InP epilayers can improve the quality of epilayers dramatically, by this means, for 2.6-μm-thick heteroepitaxial InP, the full-widths at half-maximum (FWHMs) of XRD ω and ω-2θ scans are 219 and 203 arcsec, respectively, the RT PL spectrum shows the band edge transition of InP, the FWHM is 42 meV. In addition, the successful growth of InP/$In_{0.53}Ga_{0.47}As$ MQWs on GaAs(100) substrates indicates the quality of device demand of InP/GaAs heterostructures.

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The InP-based optoelectronic devices are essential for optical communication, while InP-based integrated circuit (IC) technology is still undeveloped in comparison with that of GaAs IC. If InP-related optoelectronic devices and GaAs electronic devices are combined with GaAs substrates, optoelectronic integrated circuits (OEIC) could be obtained[1,2]. Therefore, InP epilayers grown on GaAs substrates have attracted considerable attention[3−7]. In addition, large area and low cost GaAs substrates are available compared with InP substrates.

However, there is 4% lattice mismatch of InP/GaAs heterostructure, by theoretical analysis[8], the critical thickness is lower than 5 nm, the numerous dislocations like threading and interfacial dislocations will come about after a critical film thickness is reached. Efforts have been made in pursuit of growing high quality of buffer layer to suppress the dislocations, such as the two-step method[9], sawtooth-patterned substrates[10], thermal cyclic annealing (TCA)[9]. Among them, the two-step method was commonly adopted to directly grow InP/GaAs heterostructures. In this method, an initial (typically $10-70$ nm) low-temperature (LT) buffer layer is deposited and determines the crystallinity of overall heteroepitaxial epilayers, however, it cannot further improve the crystal quality, there still lies lots of dislocations in epilayers[9]. As well known, LT buffer layers, strained layer superlattice (SLS), and annealing were commonly applied in heteroepitaxial growth, such as ZnO/Si[11], GaAs/Si[12,13]. In this paper, we used the two-step method to grow InP epilayers on GaAs(100) substrates and investigated the effects of SLS and TCA on the improvement of InP epilayers, so as to explore the best scheme of InP/GaAs(100) growth for OEIC applications.

Low-pressure (LP) metalorganic chemical vapor deposition (MOCVD) system was employed in the epitaxial growth, the chamber pressure was 100 torr, trimethyl-indium (TMIn), trimethyl-gallium (TMGa), and phosphorus (PH_3) were used as source materials. The carrier gas was palladium-diffused H_2 and the flow rate was 6.0 L/min.

InP/GaAs(100) heterostructures were characterized by double crystal X-ray diffraction (XRD) and room temperature (RT) photoluminescence (PL). XRD measurements were performed with Cu-$K_{\alpha 1}$ radiation source ($\lambda = 0.15405$ nm) in the InP(004) reflection, the RT PL spectra were measured by the 532-nm line of YAG laser.

As shown in Fig. 1, firstly the initial LT InP layers which had the same thickness of 35 nm were grown on GaAs(100) substrates, the V/III growth ratio was 200 and the temperature varied from 350 to 550 °C, then InP epilayers were grown on these buffer layers respectively, the subsequent InP epilayers were 1 μm thick at 685 °C with 150 of V/III ratio.

Figure 2 shows the full-widths at half-maximum (FWHMs) of XRD ω scans of 1-μm InP epilayers in the InP(004) reflection at different LT InP temperatures, they are 683, 656, 632, 667, 693 arcsec, respectively, it has the lowest value with LT InP grown at 450 °C. Therefore,

InP epilayer 1 μm, 685 °C
InP LTB layer $5-70$ nm, $350-550$ °C
GaAs substrate

Fig. 1. Growth scheme of InP epilayer on GaAs(100) substrates with various buffer layers by the two-step method.

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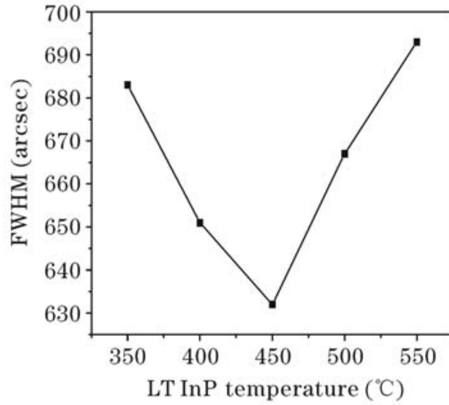

Fig. 2. Dependence of FWHM of the XRD ω scans of 1-μm epilayers on LT InP temperature.

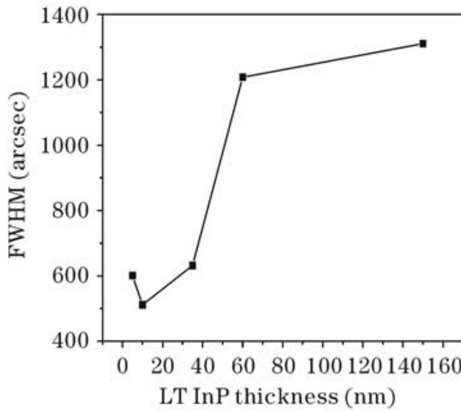

Fig. 3. Dependence of FWHM of the XRD ω scans of 1-μm epilayers on LT InP thickness.

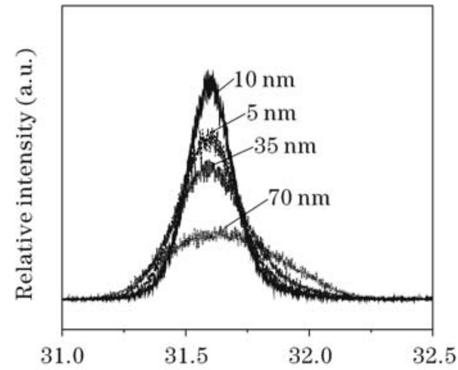

Fig. 4. XRD ω scans of 1-μm InP epilayers on 5-, 10-, 35-, 70-nm-thick LT InP layers.

we employed 450 °C for the initial LT InP growth and varied its thickness, the growth conditions of InP epilayers were the same. The FWHMs of XRD ω scans with different LT InP thicknesses are shown in Fig. 3, they are 601, 512, 632, 1208, 1311 arcsec, respectively, when the LT InP thickness is 15 nm, the FWHM is minimum. Figure 4 shows the corresponding XRD ω scans, we can see that the effects of LT InP thickness on the quality of epilayers are quite obvious.

Therefore, the optimized growth conditions for LT InP is temperature of 450 °C and thickness of 15 nm. Then we prepared samples listed in Table 1, InP epilayers were all grown at 685 °C and 1.2 μm thick totally. Three times of TCA were performed in PH_3 and H_2 ambient, the samples were heated to 750 °C and stabilized for 5 min and cooled to 300 °C in each cycle, 10 periods of 5-nm $Ga_{0.1}In_{0.9}P$/5-nm InP SLS were located in different positions of InP epilayers and also grown at 685 °C, LT GaAs was 50-nm thickness grown at 450 °C. The FWHMs of XRD ω-2θ and ω scans in the InP(004) reflection and RT PL were listed in Table 1. It shows that LT GaAs has a bit effects on InP's quality (sample 1 via sample 2), therefore, the other samples were all grown with LT

Table 1. Heteroepitaxial Growth Scheme of 1.2-μm InP on GaAs(100) by the Two-Step Method with TCA and 10 Periods of $Ga_{0.1}In_{0.9}P$/InP SLS

No.	Growth Scheme	XRD FWHM (arcsec)		PL FWHM
		ω-2θ Scan	ω Scan	(meV)
1	InP(1.2 μm)/LT InP/GaAs Substrate	406	483	
2	InP(1.2 μm)/LT InP/LT GaAs/ GaAs Substrate	373	476	47.3
3	TCA/InP(1.2 μm)/LT InP/LT GaAs/GaAs Substrate	363	412	
4	InP(1.1 μm)/SLS/InP(0.1 μm)/LT InP/LT GaAs/GaAs Substrate	392	381	
5	InP(0.6 μm)/SLS/InP(0.6 μm)/LT InP/LT GaAs/GaAs Substrate	486	402	
6	InP(0.9 μm)/SLS/InP(0.3 μm)/LT InP/LT GaAs/GaAs Substrate	325	371	46.0
7	TCA/InP(0.9 μm)/SLS/InP(0.3 μm)/LT InP/LT GaAs/GaAs Substrate	333	372	

Table 2. Heteroepitaxial Growth Scheme of 2.6-μm InP on GaAs(100) by the Two-Step Method without and with TCA or 10 Periods of $Ga_{0.1}In_{0.9}P$/InP SLS, as Well as Their Corresponding FWHMs of XRD and PL Measurements

No.	Growth Scheme	XRD FWHM (arcsec)		PL FWHM
		ω-2θ Scan	ω Scan	(meV)
8	InP(2.6 μm)/LT InP/LT GaAs/GaAs Substrate	264	295	42.3
9	TCA/InP(2.6 μm)/LT InP/LT GaAs/GaAs Substrate	238	267	
10	InP(2.3 μm)/SLS/InP(0.3 μm)/LT InP/LT GaAs/GaAs Substrate	203	219	41.8

GaAs firstly. Obviously, TCA (sample 3) and SLS (sample 6) all have distinct effects on improving epilayer's quality, but SLS must be placed in proper position in InP epilayers (samples 4 and 5 via sample 6). It is believed that TCA is very effective in reducing threading dislocation density in InP/GaAs growth[9], and SLS can effectively prevent threading dislocations up to epilayer surface[14]. Compared with TCA, the effects of SLS are more obvious (sample 6 via sample 3), however, the quality of InP epilayer with both SLS and TCA (sample 7) can hardly be improved. In addition, performing TCA is time-consumed very much; therefore, its significance for OEIC applications is little compared with SLS.

To investigate the effects of three times of TCA and 10 periods of $Ga_{0.1}In_{0.9}P$/InP SLS on InP epilayers with thicker thickness, in Table 2, InP epilayers were increased to 2.6 μm. Figure 5 shows their XRD ω-2θ scans in the InP(004) reflection, each has two peaks, the right one is produced by GaAs substrates and the left one corresponds to InP epilayers. $\Delta\theta$ between both peaks is related to the lattice mismatch parameter $(\Delta a/a)_\perp$ between InP and GaAs along the growth direction, the arrow shows the expected angular position in the case of strain-free InP epilayers, indicating there exists compressive strains in InP epilayers. Obviously, the XRD FWHM of InP epilayers is related to their thickness, they all have a dramatically decrease, and are 264 and 203 arcsec for samples with and without SLS, 238 arcsec for TCA sample. Figure 6 shows the corresponding ω scans in Fig. 5, which were commonly used to estimate the crystalline quality, the values of 295, 267, 219 arcsec correspond to a crystal of good quality by the two-step method[5,15], similarly, it indicates that 10 periods $Ga_{0.1}In_{0.9}P$/InP SLS has improved the quality of InP epilayer more obviously than TCA. In Fig. 7, we give a comparison of the RT PL spectra for InP epilayer with and without SLS for samples in Table 2, the central position of 915 nm corresponds to the band edge emission of InP at RT, in the same excitation density, the sample with SLS has a stronger relative intensity than that of the sample without SLS, their FWHMs are almost the same of 42 meV.

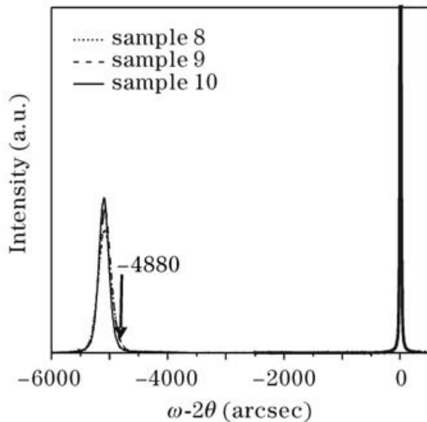

Fig. 5. XRD ω-2θ scans of InP/GaAs(100) heterostructures in the InP(004) reflection.

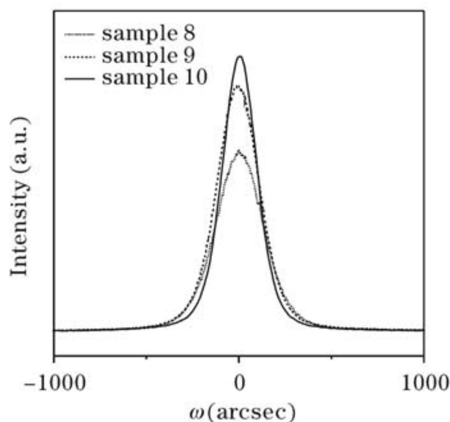

Fig. 6. Corresponding XRD ω scans in InP(004) reflection for samples in Fig. 5.

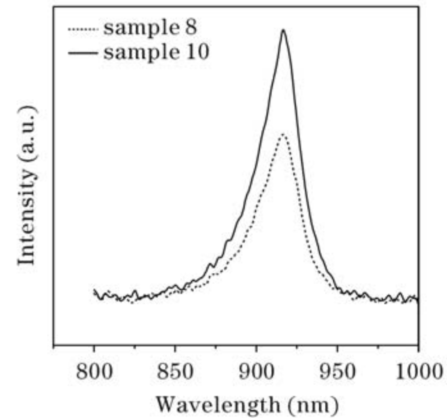

Fig. 7. RT PL spectra of InP/GaAs(100) heterostructures with or without SLS in InP epilayers for samples in Table 2.

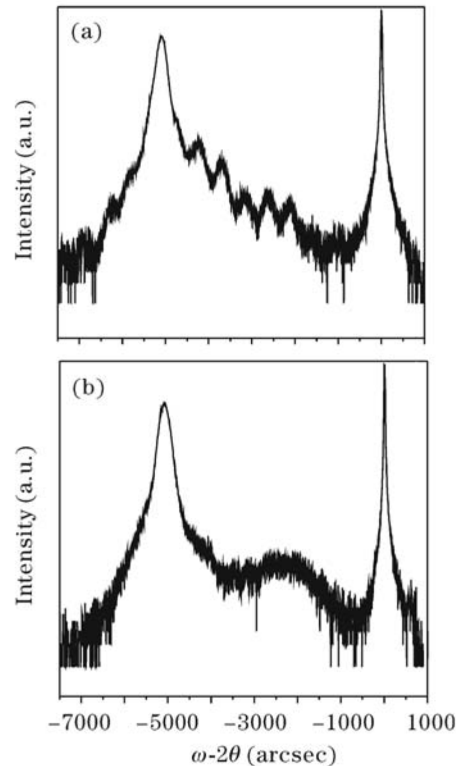

Fig. 8. XRD ω-2θ scan for 10 periods of InP/$In_{0.53}Ga_{0.47}$As MQWs on InP/GaAs(100) substrates (a) with or (b) without SLS used in improving the quality of InP eipilayers.

To test the application of our samples, we attempted to grow 10 periods of 20-nm InP/15-nm $In_{0.53}Ga_{0.47}As$ multiple quantum wells (MQWs) on InP/GaAs(100) heterostructures, which were commonly used in LED and LDs devices as emission layers. We grew two samples, one used SLS to improve the quality of InP/GaAs heterostructrue and the other did not, each sample was grown in one run. Figure 8 shows the XRD ω-2θ scan for the MQWs on InP/GaAs(100) heterostructure with SLS, in Fig. 8(a) the left peaks are from InP/$In_{0.53}Ga_{0.47}As$ MQWs, the satellite peaks can be differentiated distinctly, the angular separation between satellites is about 1060 arcsec, by diffraction theory of multiple layers[16], and the calculated period thickness is about 35 nm, as we know presently, MQWs on InP/GaAs(100) heterostructures were seldom reported and showed satellite peaks by XRD[17]. The successful growth of InP/$In_{0.53}Ga_{0.47}As$ MQWs on GaAs(100) substrates shows that the quality of our heterostructures can basically satisfy the need of optoelectronic device demanded. As a comparison, Fig. 8(b) shows almost no satellite peaks.

In conclusion, by the two-step method we grew InP epilayers on GaAs(100) substrates, the growth conditions of LT InP were optimized, 450 °C and 15 nm were found to be the optimum growth conditions for LT InP in growing InP/GaAs heterostructures. To further improve the quality of our samples, the effects of LT GaAs, three times of TCA and 10 periods of 5-nm $Ga_{0.1}In_{0.9}P$/5-nm InP SLS on the quality of InP epilayers were investigated, it was found that 10-period $Ga_{0.1}In_{0.9}P$/InP could obviously improve the quality compared with TCA. Therefore, combined with the two-step method, the optimum growth scheme for InP/GaAs(100) heterostructures was obtained, for a 2.6-μm-thick sample, the FWHMs of XRD ω scan and PL were only 219 arcsec and 42 meV, respectively, indicating high quality of our sample. In addition, InP/$In_{0.53}Ga_{0.47}As$ MQWs were attempted to grow on InP/GaAs(100) heterostructures, the XRD ω-2θ scan shows distinct satellite peak. The successful growth of InP/$In_{0.53}Ga_{0.47}As$ MQWs on GaAs(100) substrates indicates the quality of optoelectronic device demand of InP/GaAs heterostructures.

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