Design and numerical analysis for low birefringence silica on silicon waveguides

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A new fabrication technology for three-dimensionally buried silica on silicon optical waveguide based on deep etching and thermal oxidation is presented. Using this method, a silicon layer is left at the side of waveguide. The stress distribution and effective refractive index are calculated by using finite element method and finite different beam propagation method, respectively. The results indicate that the stress of silica on silicon optical waveguide fabricated by this method can be matched in parallel and vertical directions and stress birefringence can be effectively reduced due to the side-silicon layer.

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While planar optical waveguides in silica have shown enormous promise for wavelength routing application, a problem is proposed due to their birefringence. It is thought to come from the use of a silicon substrate, which strains the glass layer because of its different expansion coefficient after the sintering or annealing of the glass layer. This birefringence must be reduced substantially before this kind of optical waveguide is practically introduced. Several approaches have been reported for eliminating the stress birefringence in planar lightwave circuits[1−4]. This letter describes a new method for fabricating low birefringence silica-based optical waveguide. Stresses of silica waveguide with a side-silicon layer are examined by using finite element method (FEM). At the same time, effective refractive indices are calculated by using finite different beam propagation method (FD-BPM).

The fabrication processes for buried silica on silicon optical waveguide are shown in Fig. 1. The first step is to etch silicon wafer directly by reactive ion etching (RIE) to form waveguide space. The waveguide space is about 22.8 μm in order to get sidecladding with 15-μm thickness after thermal oxidation and leave core with 6 μm width. The gaps between two waveguides and the depths are not less than 36 and 29.4 μm, respectively. Furthermore, these values should be optimized. For the second step, the silicon wafer was oxidized for thirty days under the hydrosphere atmosphere at 1050 °C. The obtained SiO_2 layer is about 15 μm thick, which is named as undercladding and sidecladding. And a silicon layer is left between waveguides, which is named as side-silicon layer. The third step is to deposit two successive glass particle layers using flame hydrolysis deposition (FHD) or plasma enhanced chemical vapor deposition (PECVD). It forms a core of 6-μm thickness together with an overcladding of 15-μm thickness. Finally, the substrate with these two porous glass layers is heated to about 1000 °C for consolidation or annealing. Using this new method, the side-silicon layer with higher thermal expansion coefficient can be remained between two waveguides, in which the width and depth are marked as w and d, respectively, as denoted in Fig. 1.

FEM is used[5] to calculate the stresses in the core structure, and the geometrical and mechanical parameters of each layer are specified. Some involved parameters, including thermal expansion coefficient, Poisson's ratio, and Young's modulus, are listed in Table 1 for

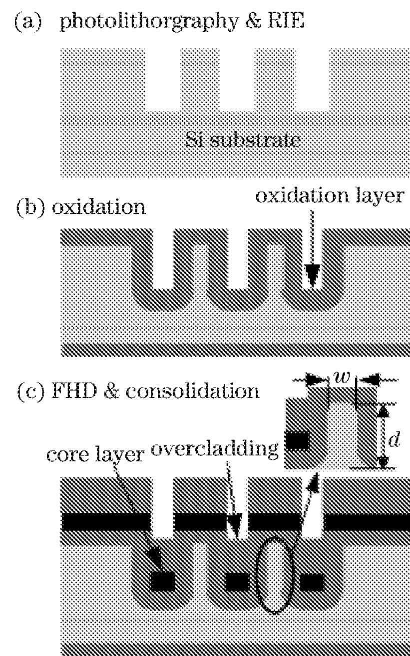

Fig. 1. Fabrication processes of optical waveguide.

Table 1. Mechanical Data Used in Strain Calculations: Young's Modulus (E), Poisson's Ratio (ν), and Thermal Expansion Coefficient (α) for Si, SiO_2 Cladding and Core

	Si	SiO_2 Cladding	SiO_2 Core
E ($\times 10^9$ Pa)	131	65	70
ν	0.28	0.17	0.2
α ($\times 10^{-6}$ K^{-1})	3.6	0.5	1.2

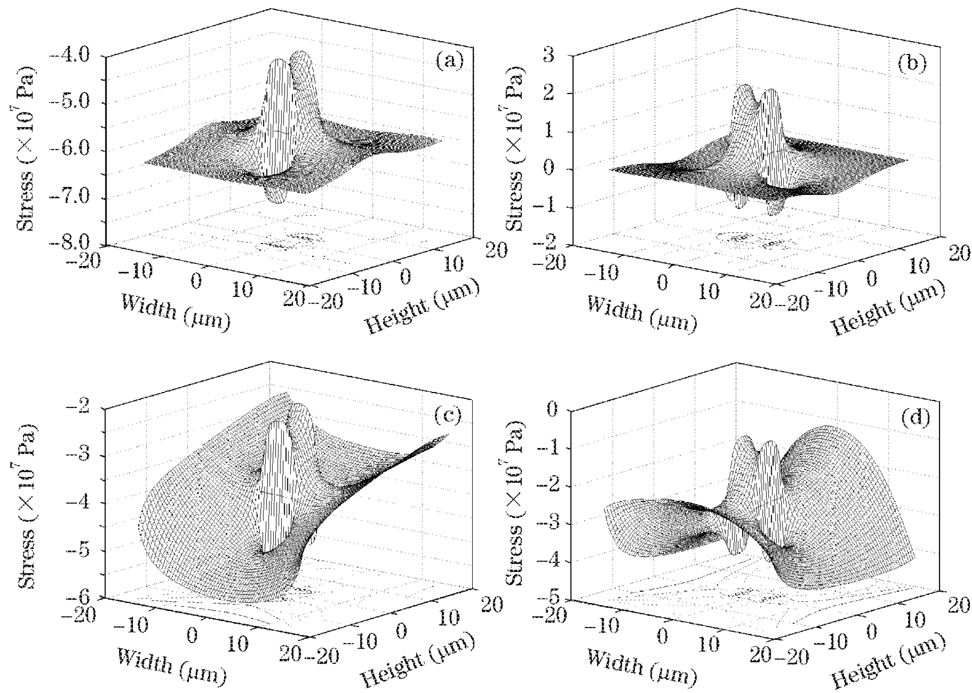

Fig. 2. The stress distribution in parallel and perpendicular to the wafer surface. (a): Parallel to the wafer surface with w = 0 μm; (b): perpendicular to the wafer surface with w = 0 μm; (c): parallel to the wafer surface with w = 10 μm, d = 36 μm; (d): perpendicular to the wafer surface with w = 10 μm, d = 36 μm.

the Si, SiO_2 cladding and core layers, respectively[6,7]. Here all the materials are assumed to be mechanically isotropic. Subsequently, the model is split into a mesh of elements and the strain components of each element are calculated. The elements were defined to be smaller near the optical waveguide than those far from it. The cross section area modeled here was 300×2000 μm^2, which included three cores, each with area 6×6 μm^2.

The changes of the refractive index for triaxial stresses in a Cartesian coordinate system are

$$\Delta n_x = n_x - n = -B_2\sigma_x - B_1(\sigma_y + \sigma_z), \qquad (1)$$

$$\Delta n_y = n_y - n = -B_2\sigma_y - B_1(\sigma_x + \sigma_z), \qquad (2)$$

where the stress optical coefficients $B_1 = 4.2\times10^{-12}$ Pa and $B_2 = 6.5\times10^{-13}$ Pa[8], refractive index n = 1.444, and the refractive index difference between core and cladding is 0.75%. The propagation constant is calculated based on the refractive index output from stress analysis by full-vector alternating direction implicit (ADI) iterative method[9]. Then the birefringence index $B = (\beta_{\rm TM} - \beta_{\rm TE})/k_0$.

Figure 2 shows the calculated stress distribution near one optical waveguide in parallel and perpendicular to the wafer surface, where Figs. 2(a) and (b) are corresponding to the case without side-silicon layer, and Figs. 2(c) and (d) to the case with the side-silicon layer of 10-μm width and 36-μm depth. When no side-silicon layer exists, in parallel to the wafer surface, one finds the expected compressive stress resulted from the higher thermal expansion of the substrate silicon. While in perpendicular to the wafer surface, one finds the core is suffered from expansive stress and the cladding is not suffered from it almost, which results in higher stress difference between the cases of parallel and perpendicular to the wafer. But comparing with Figs. 2(a) and (b), (c) and (d) shows that the waveguide is suffered from significant compressive stress in not only parallel, but also perpendicular to the wafer surface, arising from the existence of the side-silicon layer. It means that the stresses in parallel and perpendicular to the wafer can be matched well with each other. This is the reason for resulting in very low stress difference between two directions.

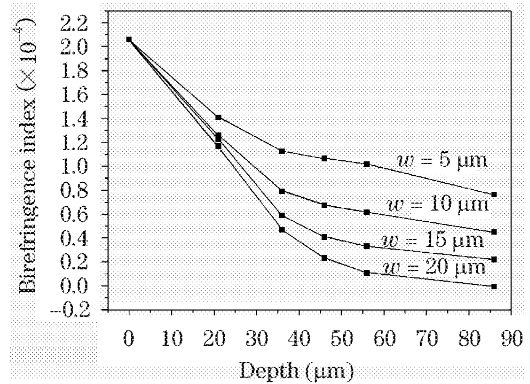

Fig. 3. Calculated birefringence as a function of the depth and width of silicon at the side of waveguide.

Stress-birefringence index calculated by FD-BPM is shown in Fig. 3. The results indicate that the waveguide birefringence can be reduced effectively due to the existence of the side-silicon layer and the reduced quantity depends on the depth and width of this layer. For a given silicon layer width w, the birefringence index decreases faster at d < 36 μm than at d > 36 μm. For a given silicon layer depth d, a larger width of the side-silicon

layer helps to reduce the birefringence. The result indicates that, by optimizing w and d, the birefringence index can be lowered to 1.0×10^{-4}, which meets the demand of the low birefringence optical waveguide devices such as arrayed waveguide grating (AWG), Mach-Zehnder interferometer, and so on.

We have presented a novel technology for fabricating buried silica optical waveguide using deep etching and thermal oxidation technology. Based on this technology, a side-silicon layer between waveguides is left. Numerical analysis indicates that this kind of waveguide owns a very low birefringence after optimizing the width and depth of the side-silicon layer, which can be used to fabricate polarization insensitive AWG or Mach-Zehnder interferometer. Further experiment is being carried out.

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