中国激光

微米银焊点的超快激光图形化沉积及其在芯片连接中的应用探索

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摘要 集成电路(IC)芯片封装中小尺寸、细节距焊点采用的传统锡基钎料在服役过程中存在桥接、电迁移、金属间化合物等问题，在大电流、大功率密度的应用中受到限制。采用脉冲激光沉积（PLD）技术，在覆铜陶瓷（DBC）基板上图形化沉积了多孔微米银焊点，用于替代传统的钎料凸点，并将其应用于 Si 芯片与 DBC 基板的连接。结果表明：采用不锈钢作为掩模，可沉积出 500 μm 及 300 μm 特征尺寸的疏松多孔银焊点阵列，银焊点呈圆台形貌；在 250 ℃温度、2 MPa 压力下热压烧结 10 min，Si 芯片与 DBC 基板连接良好，连接后的银焊点边缘的孔隙率为 42% 左右，银焊点中心区域的孔隙率为 22%；500 μm 和 300 μm 特征尺寸的银焊点的连接接头的剪切强度分别为 14 MPa 和 12 MPa；接头断裂主要发生在银焊点与芯片或 DBC 基板的连接界面处。

关键词 激光技术；脉冲激光沉积；图形化连接；多孔微米银焊点；热压烧结；剪切强度

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1 引 言

随着电子封装技术向小型化和集成化方向的不断发展，人们对电子器件中芯片的电能和热能转移提出了更高要求[1]。目前集成电路芯片中的球栅阵列(Ball Grid Array，BGA)、倒装芯片互连焊点等主要采用锡基钎料，以实现芯片及基板间的机械支撑和电气互连。但受制于锡球本身的物理及化学性能，芯片焊点在大功率、高热流密度工况下长时间服役时，会出现桥接、电迁移、金属间化合物生长等各种问题[2-3]，因此开发新型焊接材料及其连接工艺迫在眉睫[4-5]。

近年来，以纳米银、铜等为代表的纳米金属焊膏凭借其尺度效应已实现低温焊接[6-11]，正受到电子封装领域的关注[12-15]。纳米金属颗粒烧结后的性能与块状金属相当，具有较高的电导率和导热系数，在芯片焊接中具有广阔的应用前景[16-18]。其中，纳米银焊膏具有较低的烧结温度、较强的抗腐蚀和抗氧化性能，目前已经进入商业化阶段[19-20]；纳米铜焊膏较银膏具有价格优势，电迁移率低且稳定性好，具有潜在的应用价值[21-24]，但其易氧化且烧结温度高[25]。此外，纳米金属焊膏中有机物的存在使得烧结过程复杂，降低了生产效益[26-28]；同时烧结接头中有机物分解不充分而产生的空洞也会造成接头性能和可靠性的降低[29]。

脉冲激光沉积(Pulsed Laser Deposition，PLD)[30-33]是一种通过物理方法制备金属纳米颗粒及薄膜的工艺。激光直接烧蚀靶材产生的金属纳米颗粒，均匀溅射在基板表面。该技术制备的纳米颗粒及薄膜无有机物有望替代纳米焊膏并应用于电子封装中。目前，Feng 等[31]采用 PLD 技术制备了一种无有机物且可长期存储的疏松-致密双层纳米 Ag 互连材料来实现器件连接，结果显示，疏松层具有大变形能力，致密层具有良好的界面连接能力。Zubir 等[32]将制备的 PLD-Ag 颗粒材料应用于大面积芯片连接，连接层未见空洞、裂纹等缺陷，接头剪切强度高。

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Wang 等[33]采用 PLD-Ag 膜连接 SiC 芯片与覆铜陶瓷基板，发现 180 ℃连接接头的剪切强度可达 18 MPa。王文淦等[34]采用 PLD-Ag 微纳颗粒复合薄膜在 250 ℃温度下连接了 SiC 芯片与覆铜陶瓷(DBC)，300 ℃保温 2000 h 后的剪切强度高于 20 MPa。贾强等[35]采用 PLD 工艺制备的 Ag-Pd 纳米合金颗粒连接 SiC 芯片及 DBC，其抗电迁移能力是同等条件下纯 Ag 纳米颗粒的 4.3 倍。以上研究均是采用 PLD 技术在芯片上整面沉积纳米颗粒薄膜，并应用于功率电子器件的芯片封装。对于应用范围更广的集成电路芯片封装，大多需要在特定微小区域中制备具有特定尺寸和节距的凸点阵列来实现芯片与基板的互连，因此探索 PLD 制备图形化微凸点阵列技术并用金属纳米颗粒薄膜取代传统锡球和焊膏，对于集成电路芯片的封装具有重要的理论意义和工程应用价值。

为了制备具有特定尺寸和节距的由金属纳米颗粒组成的微凸点阵列，本文首先采用超快激光加工出具有图形化阵列孔的不锈钢掩模，然后用 PLD 工艺图形化沉积微米银焊点阵列，最后将沉积的图形化微米银焊点应用于芯片与基板的倒装互连。本文研究了 PLD 图形化沉积微米银焊点的形貌特征，分析了芯片-基板连接接头的微观组织，并对接头的剪切强度和断裂类型进行了评估，探索了 PLD 图形化沉积微米银焊点在集成电路芯片封装中应用的可行性。

2 试 验

2.1 试验设备和材料

试验中 Si 芯片型号为 JZDN11020-1P（尺寸为 0.33 mm×9.8 mm×9.8 mm），表面镀有 Ti/Ni/Ag 金属化层。基板材料为表面镀有 Ni/Au 金属化层的 Al_2O_3 陶瓷覆铜板，尺寸为 20 mm×20 mm。PLD 图形化沉积采用的掩模材料为聚酰亚胺(Polyimide，PI)胶带粘接层+304 不锈钢，掩模尺寸为 17.5 mm×17.5 mm。PI 胶带由粘接层和离尘膜构成，使用时将离尘膜揭去，粘接层厚度为 50 μm，不锈钢的厚度分别为 50，30，20，10 μm，故 4 种掩模的总厚度为 100，80，70，60 μm。激光加工的掩模孔的直径即 PLD 图形化沉积银焊点的特征尺寸为 500，300，200 μm，掩模孔阵列中相邻掩模孔的圆心距(节距)为特征尺寸的 2 倍，每平方厘米所需加工的掩模孔的数目分别为 100、256 和 625，每平方厘米面积上掩膜孔所占的理论有效面积为 19.6%。

2.2 微米银焊点的图形化沉积

图1为PLD图形化沉积工艺流程示意图。首

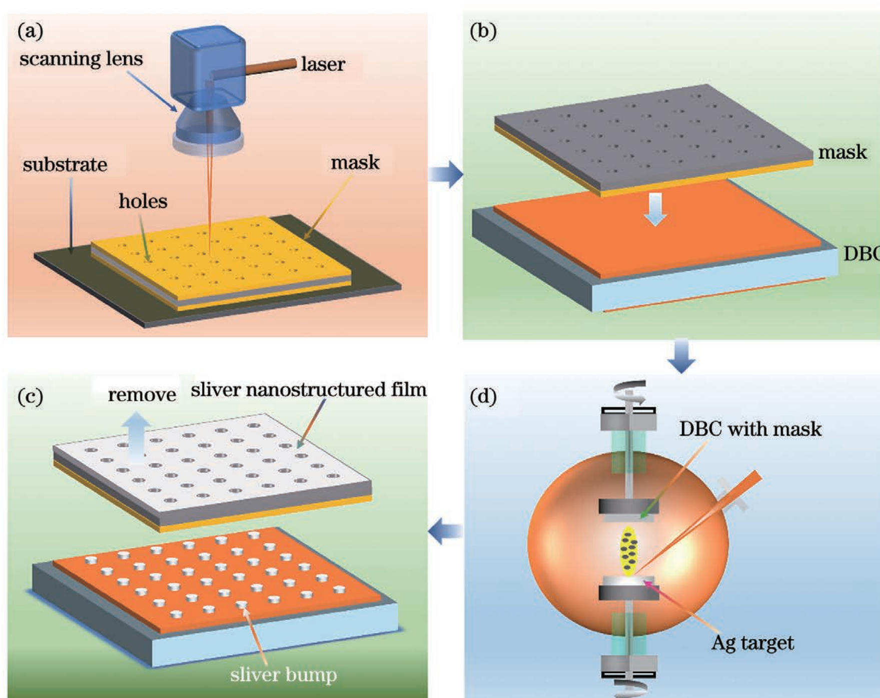

图 1 图形化沉积微米银焊点工艺过程。(a)激光加工不锈钢掩模；(b)掩模粘贴 DBC 基板；(c)PLD 图形化沉积；(d)沉积的微米银焊点

Fig. 1 Patterning deposition process of micron sliver bumps. (a) Laser machined stainless steel mask; (b) mask pasted to DBC substrate; (c) PLD patterning deposition; (d) deposited micron sliver bumps

先,将 PI/不锈钢/PI 的三明治结构粘贴在表面光滑的不锈钢基板上,采用 Edgewave PX100-2-GH 型皮秒激光器在总面积为 15 mm×15 mm 的区域加工掩模孔阵列(为了防止掩模过度烧蚀,激光功率为 1 W 左右);去除底层 PI 粘接层并超声清洗;用上层 PI 胶带将不锈钢掩模紧密粘贴在 DBC 基板上,如图 1(b) 所示;然后利用皮秒激光(沉积功率为 70 W)烧蚀银靶产生纳米银颗粒,颗粒通过掩模孔沉积在 DBC 基板上,如图 1(c)所示,沉积在 500 Pa 氩气气氛中进行[33];最后去除不锈钢掩模即可得到由疏松纳米银颗粒组成的微米银焊点阵列。

上述工艺过程中掩模的制备、粘贴步骤复杂,实际应用中的可操作性差。在实际应用中,晶圆图形化采用光刻胶作为掩模材料,通过光刻工艺制备出图形化掩模孔,然后通过 PLD 工艺在晶圆上沉积纳米颗粒薄膜,最后去除光刻胶掩模,即可得到图形化的焊点阵列。

2.3 芯片-DBC 的热压连接

微米银焊点沉积完成后,芯片与基板的热压连接过程在空气中进行,芯片在使用前用乙醇擦拭表面。图 2(a)为接头热压连接示意图,图 2(b)为热压连接过程中的温度变化曲线,升温阶段的加热速率为 25 ℃/min,在 250 ℃下保温 10 min 后空冷至室温。整个过程中恒定施加 2 MPa 的压力,根据理论有效连接面积计算 Si 芯片与 DBC 基板在热压连接过程中的压力大小。

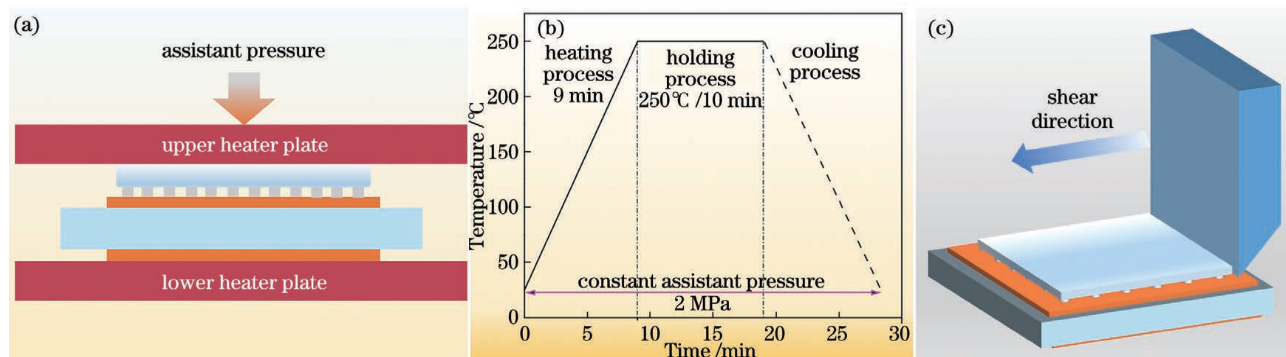

图 2 芯片-DBC 热压连接及其剪切测试。(a)芯片-DBC 的热压连接示意图;(b)烧结温度曲线;(c)芯片-DBC 接头的剪切强度测试示意图

Fig. 2 Chip-DBC hot pressing bonding and its shear test. (a) Schematic of chip-DBC hot pressing bonding; (b) sintering temperature curve; (c) schematic of chip-DBC joint shear strength test

2.4 表征手段

采用 LEXT OLS4500 激光共聚焦显微镜观察沉积得到的微米银焊点的三维形貌。用 Dage 4000 拉力剪切力测试仪测定芯片-DBC 连接接头的剪切强度,图 2(c)为剪切强度测试示意图。推剪力测试范围为 0～100 kg,剪切速度为 100 μm/s。每种尺寸的微米银焊点对应测试 5 个接头,剪切强度取 5 个接头强度的平均值。为了观察芯片-DBC 接头的连接界面形貌,先对芯片进行切割,然后用碳化硅防水砂纸进行打磨,并采用 Leica EM TIC 3X 型离子抛光机对截面进行抛光。采用 Merlin Compact 型扫描电子显微镜(Scanning Electron Microscope,SEM)对沉积银焊点的形貌、接头的截面和断口表面形貌进行表征。接头截面组织的孔隙率由 Image J 软件计算。

3 分析与讨论

3.1 PLD 图形化沉积微米银焊点形貌

图 3 为三种特征尺寸银焊点阵列的沉积形貌,包括焊点宏观形貌、共聚焦显微镜采集的焊点三维形貌及采用不同厚度掩模的焊点中心截面高度的变化曲线。图 3(a)、(b)为 500 μm 特征尺寸银焊点形貌及组成银焊点的纳米颗粒形貌,60 μm 高度的银焊点的顶部平台直径约为 330 μm。由纳米颗粒的形貌可知,组成焊点的纳米银颗粒的粒径主要在几十至几百纳米之间,且纳米颗粒随机分布,这与文献[33]的研究结果吻合。图 3(d)、(e)为 300 μm 特征尺寸银焊点的形貌特征,50 μm 高度的银焊点的顶部平台直径约为 100 μm。以上两种特征尺寸的银焊点均表现出底部大、顶部小的圆台形貌,且焊点形貌及尺寸规则统一。沉积过程中激光功率与沉积参数的稳定性、基板上不同位置沉积厚度的均一性等因素造成了两种特征尺寸焊点沉积高度的差异。图 3(g)、(h)为 200 μm 特征尺寸银焊点的形貌特征,焊点呈圆锥状,焊点高度为 45 μm,已达当前沉积参数下的最大高度,且部分焊点的形貌有明显缺陷。

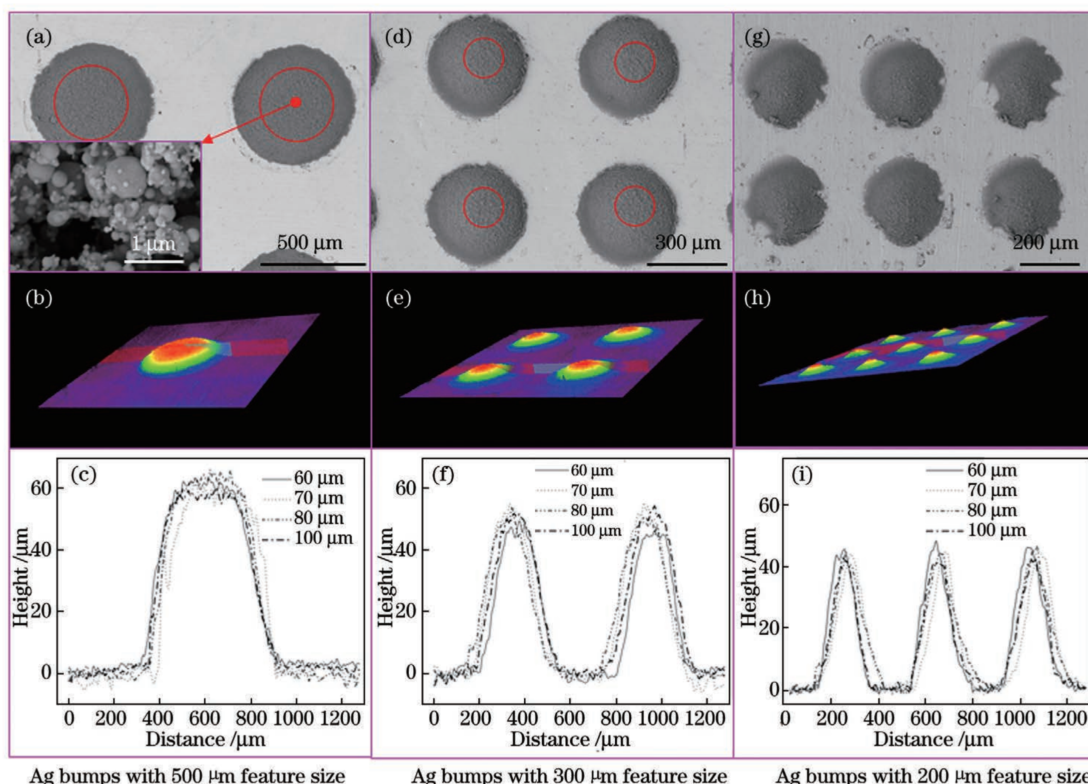

图 3　PLD 图形化沉积银焊点的形貌。(a)(d)(g)银焊点的 SEM 宏观形貌；(b)(e)(h)银焊点的共聚焦三维形貌；(c)(f)(i)不同掩膜厚度下银焊点的中心截面高度曲线

Fig. 3　Morphologies of Ag bumps by PLD patterning deposition. (a)(d)(g) SEM macroscopic morphologies of Ag bumps; (b)(e)(h) confocal three-dimensional morphologies of Ag bumps; (c)(f)(i) height variation curves of Ag bump central sections under different mask thicknesses

图 3(c)、(f)和(i)为银焊点中心截面的高度变化曲线，不同线型分别代表采用不同厚度掩模时的银焊点高度变化曲线，为了消除其他沉积参数造成的影响，每种尺寸的 4 条曲线由一次沉积得到。由同一特征尺寸银焊点的 4 条高度变化曲线可知，掩模厚度的变化几乎不影响银焊点顶部尺寸和高度。顶小底大的圆台或圆锥形貌银焊点的形成，一方面是由掩模厚度即掩模孔的深度造成的，PLD 沉积过程中的纳米颗粒从不同方向抵达掩模孔，孔内壁附近的区域只能由一侧的颗粒沉积，另一侧入射的颗粒则被掩模阻挡在掩模上表面；另一方面，激光烧蚀靶材产生的熔融态纳米银颗粒附着在掩模孔内壁，掩模孔直径随着沉积层在掩模孔内壁的横向发展而逐渐减小，最终形成侧壁具有一定斜率的圆台形貌银焊点。三种特征尺寸银焊点具有相同的侧壁斜率，说明造成银焊点圆台形貌的主要原因是掩模孔沉积过程中的堵塞，焊点能达到的最大沉积高度与焊点特征尺寸正相关。200 μm 特征尺寸的银焊点形貌尚不能达到芯片键合要求。由于掩模厚度对银焊点形貌的影响较小，下文的芯片连接采用 80 μm 厚度的掩模进行银焊点阵列的沉积。

3.2　热压连接接头的截面形貌

图 4(a)为 500 μm 特征尺寸银焊点阵列连接接头的截面宏观形貌，三个厚度均匀的银焊点间隔均匀。图 4(b)为单个银焊点的截面形貌，经热压烧结后，银焊点顶部尺寸变大且连接层厚度由 60 μm 缩小为 35 μm，高度压缩率为 42%，其中芯片与银焊点间的缝隙是制样过程中金刚石砂轮切割导致的开裂。图 4(c)～(e)为图 4(b)中不同部位的局部放大图，三区域的孔隙率分别为 41%、22%、44%，银焊点边缘区域的孔隙率(约 42%)明显高于焊点中心区域的孔隙率(22%)。银焊点的圆台形貌使得银焊点边缘无法有效受压，边缘区域仍能观察到颗粒状纳米银。沉积态的纳米颗粒之间没有形成完整的连接网络，辅助压力更有利于致密烧结层的形成，更大的压力能为纳米颗粒的重新排列、颗粒间的连接、晶粒的生长和烧结颈的形成提供更大的驱动力[33,36]。银焊点中心区域为多孔网状结构，纳米银颗粒紧密接触，经热压烧结后形成烧结颈，银焊点与其上下两侧的Si芯片和DBC基板上的镀层间均形

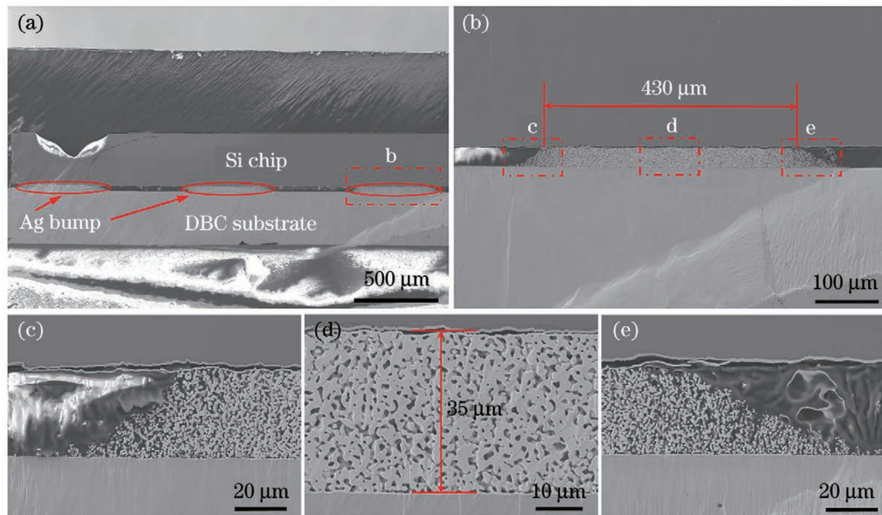

图 4 500 μm 特征尺寸银焊点阵列连接接头的截面形貌。(a)整体截面形貌;(b)单个银焊点形貌;(c)(e)银焊点的边缘形貌放大图;(d)银焊点的中心区域形貌放大图

Fig. 4 Cross-sectional morphologies of joint bonded with 500 μm feature size Ag bump array. (a) Whole sectional morphology; (b) morphology of single Ag bump; (c) (e) magnification of edge morphology of Ag bumps; (d) magnification of central-area morphology of Ag bumps

成冶金连接。此外,连接层越致密,接头的连接强度越高[33],图形化银焊点的连接强度主要由银焊点中心区域的致密连接区的连接强度提供。银柱的沉积态形貌对热压连接接头的组织、强度有较大影响,在接下来的工作中可通过改变掩模材料、PLD 沉积参数等进一步改善银柱形貌,同时进一步探索更小尺寸银柱的图形化沉积。

3.3 连接接头的剪切强度与断口形貌

剪切强度是接头性能的重要评价指标。图 5 为不同特征尺寸银焊点阵列连接接头的剪切强度。300 μm 和 500 μm 特征尺寸银焊点阵列的连接强度分别约为 12 MPa 和 14 MPa,高于美国军用标准 MIL-STD-883 K 所要求的最小强度值(～7.6 MPa)[33]。500 μm 特征尺寸银焊点阵列连接接头强度略高于 300 μm 特征尺寸银焊点,主要原因是大特征尺寸的银焊点具有更好的沉积形貌。300 μm 和 500 μm 特征尺寸银焊点在相同条件下沉积时,侧壁具有相同斜率(图 3),焊接前 500 μm 和 300 μm 特征尺寸银焊点的顶部实际连接面积分别占银焊点底部面积的 66% 和 33%,更大特征尺寸的银焊点顶部具有更大的实际有效连接面积;相反,在相同压力下,小特征尺寸银焊点在热压烧结后中心区域具有更大的致密度。烧结银焊点致密度的提高有效补偿了连接面积减小引起的强度降低;当以相同的理论有效面积计算两种特征尺寸银焊点的连接强度时,500 μm 特征尺寸银焊点的连接强度略高于 300 μm 特征尺寸银焊点。此外,由于银焊点顶部实际尺寸偏小,接头连接层的实际剪切强度高于图 5 所示强度,因此采用 PLD 工艺制备的微米银焊点替代传统的锡凸点用于电子封装,连接强度满足相关标准要求。多孔银的低弹性模量有利于芯片与基板之间形成更可靠的连接,柔度的增加可更好地适应热膨胀系数不匹配引起的应力[20,37]。

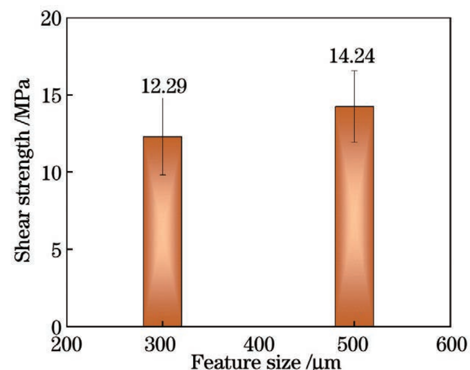

图 5 不同特征尺寸银焊点连接接头的剪切强度

Fig. 5 Shear strength of joints bonded by different feature size Ag bumps

图 6 为 500 μm 特征尺寸银焊点连接接头的剪切断口形貌。由图 6(a)、(c)可知,剪切断裂位置发生在微米银焊点与基板或芯片的连接界面处,由此可推断银焊点内部的连接强度高于银焊点与基板或芯片表面镀层界面处的连接强度。疏松的纳米银颗粒在热压烧结后形成了多孔的块体银结构,银焊点内部具有较高的连接强度;而在银焊点与芯片或基

板的连接界面处，由于热膨胀系数的不匹配，容易出现应力集中[38]。由图 6(a)可以看到，基板上残留有银焊点边缘的非致密银颗粒，结合图 4 中银焊点的截面形貌分析，可推断该圆形银焊点边缘的纳米颗粒未经有效施压而连接不紧密，而银焊点中心区域经热压烧结后颗粒间连接紧密，形成了多孔的块体银。断裂发生时，与中心区域连接不紧密的疏松银颗粒残留在 DBC 基板上，基板上残留的非致密银颗粒会对服役过程的可靠性产生一定的影响，因此还需要进一步改进银焊点的沉积形貌，减少非致密烧结银的残留。图 6(b)为基板界面断口的放大图，致密烧结银与基板的金属镀层之间通过扩散形成冶金连接，剪切时与基板相连的烧结银经过塑性变形后断裂，少量烧结银残留在基板上。图 6(d)为芯片侧界面断口的放大图，可以清晰地看出银颗粒烧结形成的网络结构，且烧结银骨架断口表面有明显的塑性变形痕迹。根据以上对断口微观组织的分析，可判断断裂为韧性断裂。对图 6(a)、(c)所示的两种凸点断裂位置进行统计，两种断裂位置随机分布，500 μm 特征尺寸凸点芯片侧的断裂个数占总体凸点的 12%左右，300 μm 特征尺寸凸点芯片侧的断裂个数占总体凸点的 76%左右。500 μm 特征尺寸焊点的有效连接面积较大，凸点与芯片的 Ag-Ag 连接界面强度高于凸点与基板的 Ag-Au 连接界面强度；而 300 μm 特征尺寸凸点顶部的实际有效连接面积与底部相差较大，致密连接区域小，连接强度低，导致大部分焊点断裂在芯片侧。

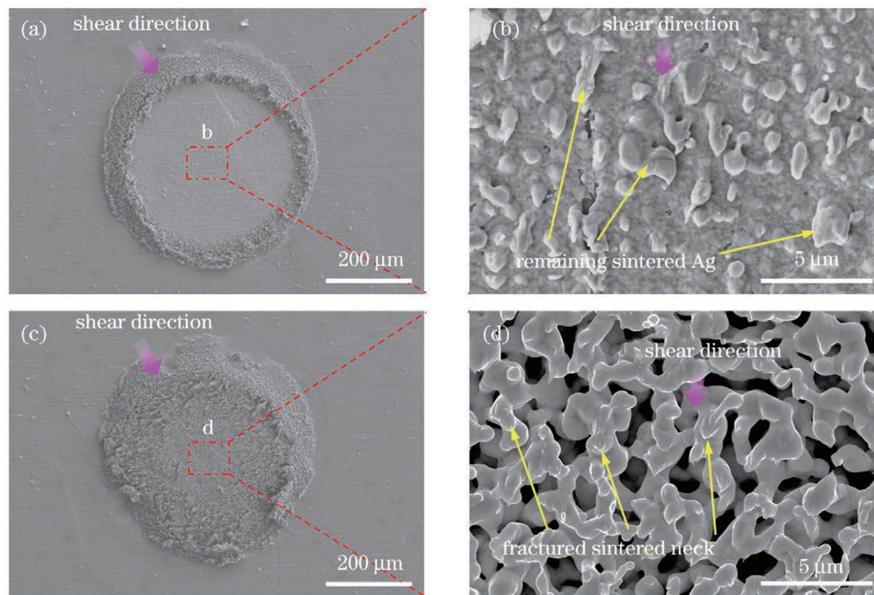

图 6 500 μm 特征尺寸银焊点阵列焊接接头的断口形貌（DBC 侧）。(a)在银焊点/DBC 基板界面处的断裂；(b)银焊点/DBC 基板断口的放大图；(c)在银焊点/Si 芯片界面处的断裂；(d)银焊点/Si 芯片断口的放大图

Fig. 6 Fracture morphologies of joints bonded by 500 μm feature size Ag bump array (DBC side). (a) Fracture occurred at Ag bump/DBC interface; (b) magnification of Ag bump/DBC fracture; (c) fracture occurred at Ag bump/Si chip interface; (d) magnification of Ag bump/Si chip fracture

图 6(a)中残留有纳米银颗粒组成的圆环，左上侧颗粒多于右下侧，在剪切断裂时，右下侧疏松的颗粒受到断裂银柱的推力作用而形成较大的坡面；同样地，图 6(c)中右下侧边缘处的少量疏松烧结银在芯片的带动下掉落。图 6(b)、(d)的断口微观形貌显示，残留的烧结银和银柱表面的烧结银在塑性变形后断裂形成的尖端均指向同一方向，故可确定接头的剪切方向。

4 结 论

采用 PLD 图形化沉积工艺制备了由纳米银颗粒组成的多孔微米银焊点，并将其应用于 Si 芯片与 DBC 基板的连接。沉积态的多孔微米银焊点呈上小下大的圆台形貌，500 μm 和 300 μm 特征尺寸的银焊点沉积 60 μm 高度时，银焊点顶部尺寸分别为 330 μm 和 100 μm。在 250 ℃、2 MPa、10 min 的热压连接参数下，银焊点与其上下两侧的芯片和基板上的金属镀层之间均形成了冶金连接，烧结后的银焊点为多孔网状组织；银焊点边缘的孔隙率为 42%左右，明显大于中心区域 22%的孔隙率。特征尺寸为 500 μm 和 300 μm 的银焊点阵列连接接头的剪

切强度分别为 14 MPa 和 12 MPa，接头断裂主要发生在银焊点与 DBC 基板或芯片的连接界面处。研究结果证明了在集成电路芯片封装中采用多孔微米银焊点替代传统焊料凸点的可行性，后续将从掩模材料和 PLD 沉积工艺等方面来改善多孔微米银焊点的形貌。

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Ultrafast Laser Patterning Deposition of Micron Sliver Bumps for Chip Bonding Application

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Abstract

Objective With the development of electronic packaging technologies towards miniaturization and integration, high requirements are put forward for the electric and heat energy transfer of chips. At present, the ball grid array (BGA) and flip-chip interconnection solder bumps in integrated circuit chips are mainly packaged with tin-based solders, which provides mechanical support and electrical interconnection between chips and substrates. However, due to the physical and chemical properties of tin balls, the problems such as bridging, electromigration, and growth of intermetallic compounds occur when the chip bumps are in service for a long time under high power and high heat flux conditions. Alternatively, the nano-metal solder pastes represented by nano silver and nano copper, can realize low-temperature bonding by virtue of their scale effect and have been attracting more and more attention in the field of electronic packaging. But the presence of organics in the nano-metal solder paste complicates the sintering process and reduces the production efficiency. Moreover, the voids caused by the insufficient decomposition of organics in the sintered joint also reduce the performance and reliability of joints. Here, we apply the pulsed laser deposition (PLD) technology, an effective method to prepare organic free silver nanostructured films, to prepare bump array with specific size and pitch. Composed of metal nanoparticles, the bumps array can be used in integrated circuit chip bonding by hot pressed sintering at low temperatures. Being a promising alternative method of traditional solder bumps, the patterned micro bump array preparation technology has important theoretical significance and engineering application value for integrated circuit chip packaging.

Methods Polyimide and 304 stainless steel are employed as mask materials here. Firstly, a sandwich structure of PI/stainless steel/PI is pasted on a flat stainless steel substrate. A picosecond laser is used to fabricate the mask hole array with a total area of 15 mm × 15 mm. Then, the underlying PI adhesive layer is removed and the mask is cleaned by ultrasound, followed by adhering the mask to the surface of direct bonding copper (DBC) substrate via the upper PI tape. After that, the PLD process is carried out in the argon atmosphere, and the nanoparticles are deposited on the DBC substrate through the mask holes. Finally, the micron sliver bump array composed of loose nanoparticles is obtained after removing the mask. The morphologic characteristics of the patterning deposited micron bump array are studied, the microstructures of the chip-substrate joints are analyzed, and the shear strength and fracture type of the joints are discussed. The feasibility that patterning deposited micron bumps are applied in integrated circuit chip packaging is evaluated.

Results and Discussions The 500 μm and 300 μm feature size Ag bump arrays with a height of about 60 μm are fabricated successfully. Due to the obstructing of the sidewall of mask holes and the gradual diameter shrinkage of mask holes caused by the accumulation of nanoparticles on the sidewall of mask holes during the deposition process, the bumps exhibit a morphology of circular truncated cone, and the top diameters of two kinds of bumps are 330 μm and 100 μm, respectively (Fig. 3). The prepared micro bumps are used to connect Si chips to DBC substrates through a hot pressed sintering process. The micron sliver bumps present a porous network structure after sintering, and the compression rate of the 500 μm bumps is 42%. Because of the special depositional morphology of the bumps, the edge area cannot be effectively compressed, resulting in a dense connection area in the central area and a loose area at the edge for each bump (Fig. 4). The joint connection strength is mainly determined by the dense connection area in the central area. The shear test results show that the shear strengths of 500 μm and 300 μm feature size

solder joints are 14 MPa and 12 MPa, respectively (Fig. 5), higher than the minimum strength value required by MIL-STD-883 K (～7.6 MPa). The joint fracture occurs at the interface between the sintered Ag bumps and the chip or DBC substrate. The fracture morphology reveals a large amount of plastic deformation of sintered silver, which can be judged as a ductile fracture (Fig. 6).

Conclusions In this paper, porous micron sliver bump arrays composed of nano-Ag particles are deposited on DBC substrates by the PLD technique to replace the traditional solder bumps, and they are applied to the connection between Si chips and DBC substrates. The results show that, by adopting stainless steel mask, Ag bump arrays with feature sizes of 500 μm and 300 μm can be deposited with a height of 60 μm and morphology of circular truncated cone, and the top diameters of two kinds of bumps are 330 μm and 100 μm, respectively. Under the thermo-compression bonding parameter of 250 ℃-2 MPa-10 min, metallurgical connections form at the upper and lower interfaces of Ag bumps with the metallized layer. The Ag bumps are transfered into a porous network structure, in which the porosity of the edge area is about 42% and that of the central area is 22%. The shear strengths of chip-DBC joints with 500 μm and 300 μm feature size Ag bump arrays are 14 MPa and 12 MPa, respectively. The joint fracture mainly occurs at the interface between the sintered Ag bumps and the chip or DBC substrate. This paper proves that it is feasible to replace the traditional solder bumps with porous micron silver bumps in the integrated circuit chip package, but it is still necessary to improve the morphology of bumps from the aspects of mask materials and PLD technology.

Key words laser technique; pulsed laser deposition; patterning bonding; porous micron sliver bumps; hot pressed sintering; shear strength